363

TF 2411

Counter

INSTRUCTION MANUAL

MP MASTER
MA23663

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MARCONI INSTRUMENTS

Size No 50632/40 ASU. GYRO DIV.

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Instruction Manual
No. EBM 2411
for

Counter

TF 2411

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1970

MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND

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Chapter 1

General information

1.1 INTRODUCTION

TF 2411 is a 50 MHz counter which offers a wide range of measurement functions.

There are three input channels; the A channel has d.c. or a.c. coupling to the input, and the sensitivity of the A channel allows signals as low as 10 mV r.m.s. to be measured.

The instrument is small and compact but the mechanical layout gives ready access to all internal components, for ease of servicing.

Extensive use is made of integrated circuits, giving increased reliability and a power consumption low enough to make a cooling fan unnecessary.

Other features include units illuminated in the front panel, automatic triggering and variable display time. The frequency range of the instrument may be increased by using it with a prescaler; and as an optional extra the measurement reading can be brought out to the rear panel to drive a printer.

A number of frequency standards, one of which must be used, are available, these standards being complete units which plug in at the rear panel of the counter. These standards give a choice of standard to suit the requirement.

Fig. 1.1 Counter TF 2411

1.2 DATA SUMMARY

RANGE:

Frequency:	0 to 50 MHz. Using the h.f. cut function there is more than 20 dB cut above 10 MHz and more than 25 dB cut above 20 MHz.
Single period:	0 to 10 MHz (h.f. cut automatically applied).
Multiple period:	0 to 10 MHz.
Scaling:	0 to 10 MHz.

Scaling factors:	10^1 to 10^8.
Time interval:	0.1 μs to 10^8 s.

PULSE PAIR RESOLUTION: 35 ns.

SENSITIVITY

Input A:	Manual trigger - 10 mV r.m.s. Auto trigger - 20 mV r.m.s. above 1 kHz. Usable below 1 kHz with reduced sensitivity.
Inputs B and C:	0.4 V peak, positive pulse. The input pulse must be at least 0.2 μs wide.

MAXIMUM INPUT

Input A:	50 V r.m.s.
Inputs B and C:	10 V peak.

ACCURACY

Frequency:	±1 count ± stability of standard frequency.
Time B-C: (pulses)	± stability of standard frequency.
Single period:	Trigger level error ± stability of standard frequency.
Multiple period: (sine)	$\frac{\text{Trigger level error}}{\text{number of periods}}$ ±1 count ± stability of standard frequency.
Trigger level error:	±3% with 10 mV input: ±0.3% with 100 mV input.

TRIGGER LEVEL: Coarse and fine trigger level controls give approximately ±1 V d.c. offset on manual.

INPUT IMPEDANCE

Input A:	1 MΩ approximately in parallel with 10 pF approximately. D.C. coupled or A.C. coupled via 0.1 μF.
Inputs B and C:	Nominally greater than 600 Ω.

DISPLAY: 7 decade in-line with memory. Decimal point and units are automatically indicated.

DISPLAY TIME:

Continuously variable from 50 ms to 5 s approximately, or held indefinitely until manually reset.

AUXILIARY OUTPUTS:

1) Time base.
Amplitude: Approximately +1.0 V peak into 470 Ω.

P.R.R. (with gate open): 0.1 Hz to 1 MHz in decade steps, for test and frequency measurement. 0.1 Hz to 10 MHz in decade steps for period and time measurements.

Multiple period scale: Input A divided by the scaling factor.

2) 10 MHz standard frequency.
A.C. coupled to output.

Amplitude: Approximately 1.0 V peak-to-peak into 1 kΩ.

Both these outputs are available on the rear panel prescaler connector.

POWER REQUIREMENTS:

95 V to 130 V or 190 V to 264 V, 45 to 60 Hz. 30 VA approximately. There is 10% regulation on the nominal mains setting.

DIMENSIONS AND WEIGHT:

Height	Width	Depth	Weight
89 mm	280 mm	254 mm	4.1 kg
($3\frac{1}{2}$ in)	(11 in)	(10 in)	(9 lb)

ACCESSORIES

Supplied:

Two free plugs, type BNC.

Optional:

1) External Frequency Standard. TM 9890.

Input frequency: Sub-harmonics of 10 MHz in the range 1 MHz to 10 MHz.

Input sensitivity: 120 mV to 25 V r.m.s.

Input impedance: 2.5 kΩ minimum.

2) 10 MHz Frequency Standard, TM 9888, (internal crystal oscillator).

Stability: Typical age rate of $\pm 2 \times 10^{-8}$ per week at constant temperature.
Temperature coefficient is $\pm 1 \times 10^{-6}$ per °C between 0 and 50 °C.

External standard: Sensitivity, 120 mV to 25 V r.m.s.
Input impedance, 2.5 kΩ minimum.

3) Internal Frequency Standard, TM 9933, (Internal crystal oven).

Stability (after 1 hour operation): Temperature, $\pm 1 \times 10^{-9}$ per 0 °C.

Supply, $\pm 5 \times 10^{-9}$ for ±10% mains supply variation.

Short term, typically $\pm 3 \times 10^{-10}$ over 5 minutes.

Age rate: $\pm 1 \times 10^{-8}$ per day after 24 hour stabilization.

$\pm 1 \times 10^{-7}$ per month after 30 days continuous operation.

The instrument will stabilize to $\pm 1 \times 10^{-7}$ in 10 minutes after 24 hour switch off.

4) Printer connector, TM 9891.

The output from this connector is 1-2-4-8 b.c.d. weighted.
'1' state: nominally 0.2 V positive.
'0' state: nominally 3.5 V positive from approximately 3.6 kΩ source.
Print command: 2 V positive pulse, 10 μs wide.
Print inhibit: > +2 V applied to printer socket pin 48.

5) Prescaler connector kit, containing 9 way McMurdo plug.

Chapter 2

Operation

2.1 PRELIMINARIES

The mains lead is a free cable fitted at one end with a female plug which connects with the instrument. When fitting a mains plug note that the colour coding of the mains cable is as follows:

Live	-	brown
Neutral	-	blue
Earth	-	green/yellow

In addition, the earth (or chassis) conductor has a yellow designation sleeve with a green circuit earth symbol, and the neutral conductor has a black sleeve with a white N.

Before connecting the instrument to the power supply, check that the transformer tappings and fuse rating are correct for the available supply voltage. The instrument is normally dispatched for use with 240 V supplies but it may be adjusted for other voltages as described in Sect. 4.4.

Ensure that one of the frequency standard plug-ins is connected at the rear of the counter.

Warm up time of the instrument from switch on is dependent on the frequency standard being used. If an external standard is used the instrument is ready immediately; warm up times and age rates for the internal standards are given in Sect. 1.2, Data Summary.

2.2 CONTROLS AND CONNECTORS

(1) FUNCTION switch. Selects the operation to be performed by the instrument.

(2) TIME BASE switch. Selects the reference frequency from the time base dividers. The frequency or time interval depends on the settings of this switch and the FUNCTION switch. Position 9 is inoperative for frequency measurements (i.e. there is no 10 MHz time base), and position 1 is inoperative for timing measurements (i.e. there are no 10 second timing units).

(3) SCALING FACTOR switch. Performs the same function as the TIME BASE switch for multiple period and scaling measurements.

(4) GATE switch. In the AUTO position the selected time base is in operation and, after counting, reset is automatic. In the OPEN position the gate is held open and the memory is disabled.

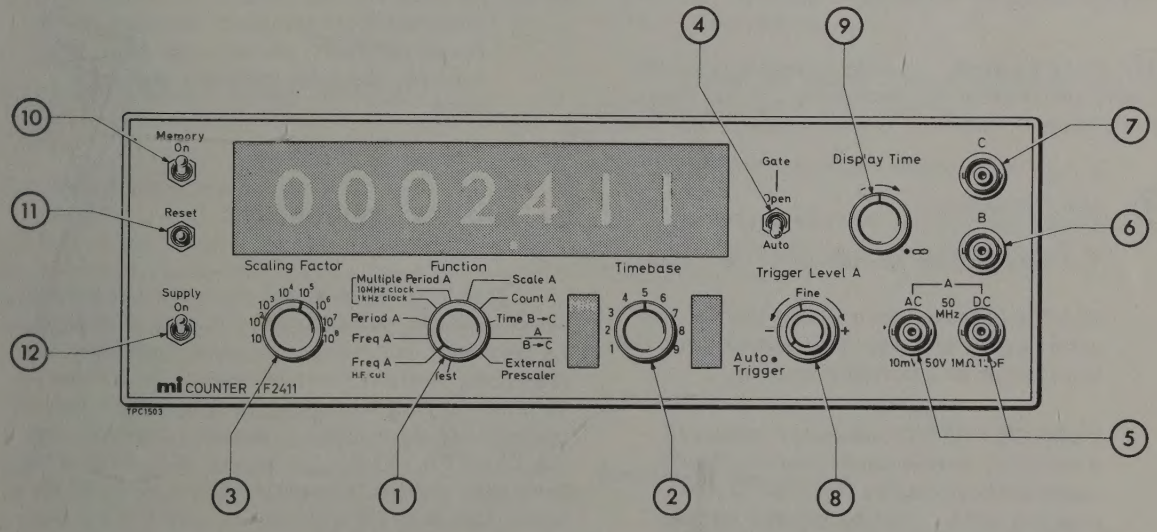


Fig. 2.1 Controls and connectors

(5) A-channel input sockets. The signal to be measured is connected to this channel for all functions except Time B-C. Use the a.c. socket for signals which have a standing d.c. in excess of ±1V.

(6) B-channel input socket. Used for time interval and A/B-C measurements. The signal fed to this input starts the counting for both measurements.

(7) C-channel input socket. Used for time interval and A/B-C measurements. This input stops the counting at the end of these measurements.

(8) TRIGGER LEVEL A controls. The outer control is for coarse adjustment and the inner for fine adjustment. Together, the controls give a manual offset of ±1V on the triggering point of A channel inputs. In the extreme counter-clockwise position the Fine control switches the instrument to automatic triggering of signals above 1 kHz and greater than 20 mV r.m.s. The coarse control is inoperative in the auto mode.

(9) DISPLAY TIME control. Adjusts the display time from about 50 ms to 5 seconds. The ∞ position holds the display until the RESET button is pressed.

(10) MEMORY switch. When set to ON, the result of one measurement is continuously displayed while the instrument is recycling; at the end of the recycling period the display changes to show the next result. The MEMORY switch is operative only when the GATE switch is set to AUTO.

(11) RESET switch. Used to manually reset the display and recycle the instrument. It will also prematurely terminate a measurement if required.

(12) SUPPLY switch.

The following are located on the rear panel:

PRESCALER connector. This carries the power supply and time base signals required to condition an external prescaler.

PRINTER OUTPUT connector (optional). A multiway socket which provides binary coded decimal outputs from the decade counting units. The socket also carries print command output, inhibit input and earth connections.

2.3 SELF CHECK

This facility allows the instrument to check the time base and decade counting units. Following installation, and from time to time, the self check facility should be used as follows:

1) Set the FUNCTION switch to TEST.

2) Set the GATE switch to AUTO, and the MEMORY switch to OFF.

3) Set the DISPLAY TIME control about quarter of a turn counter-clockwise from ∞.

4) Rotate the TIME BASE switch through its positions and observe the readouts. These should be as shown in Table 2.1 (±1 count).

Table 2.1

Time Base switch position	Readout	Units
1	000000.0	Hz
2	0000.000	kHz
3	10000.00	kHz
4	010000.0	kHz
5	0010.000	MHz
6	00010.00	MHz
7	000010.0	MHz
8	0000010	MHz
9	0000000	-

NOTE: Position 9 of the TIME BASE switch is inoperative for frequency measurements (including TEST) and although there is a readout, the units indicator window is blank.

2.4 MANUAL TRIGGERING

It is preferable to use automatic triggering where possible as this makes for ease of operation. As frequency and voltage increase, automatic triggering becomes more necessary until above 20 MHz and 20 V it must be used to ensure correct operation of the counter. Manual triggering (using the TRIGGER LEVEL A controls) will, in general, have to be used at frequencies below about 1 kHz at levels less than 100 mV r.m.s. This is particularly necessary when making period measurements and with pulse inputs.

When using manual triggering with signals above 20 MHz, the trigger level must be set with the input signal at the working voltage. Do not set the trigger level and then adjust the input level.

The method of using the manual trigger is outlined below.

For inputs below 100 mV r.m.s.:

1) Set the FUNCTION switch to FREQ A.

2) Turn the FINE control fully clockwise, and the COARSE control fully counter-clockwise.

3) Rotate the COARSE control until triggering just stops.

4) Adjust the FINE control untill triggering restarts.

5) Set the FUNCTION switch to the required measurement position, and proceed as detailed in later sections.

For inputs above 100 mV r.m.s.:

1) Set the FUNCTION switch to FREQ A.

2) Set the FINE control to mid travel.

3) Adjust the COARSE control to about the middle of the triggering band.

4) Set the FUNCTION switch to the required measurement position, and proceed as detailed in later sections.

2.5 FREQUENCY MEASUREMENT

Functional description

With the FUNCTION switch set to FREQ A, the instrument measures the frequency of a signal applied to one of the A channel input sockets by counting the number of cycles of the input over a selected interval of time.

Fig. 2.2 shows a simplified functional diagram of the instrument in this operating mode. The signal gate is opened and closed by a selected output of the time base (as selected by the TIME BASE switch). During the time that the gate is open the input signal is passed through the gate to be counted by the decade counting units.

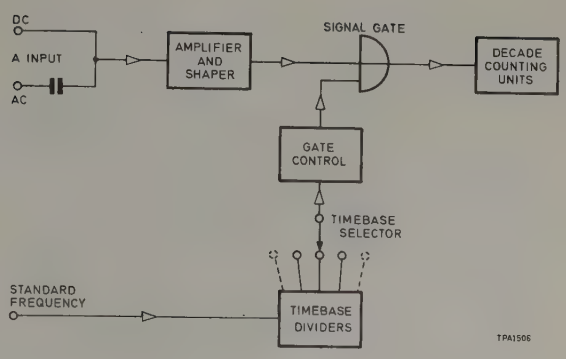


Fig. 2.2 Functional diagram: FREQ A

For frequency measurements with h.f. cut, operation is functionally the same as described above. The h.f. cut facility is useful for measuring frequencies up to 5 MHz in noise environments.

Operating procedure

Set the controls as follows:

FUNCTION switch to FREQ A (or FREQ A H.F.CUT)

TIME BASE switch to the desired frequency (note, position 9 is inoperative).

GATE switch to AUTO.

DISPLAY control and MEMORY switch as required.

TRIGGER LEVEL A, FINE control to AUTO TRIGGER. If manual triggering is required, see Sect. 2.4 for details.

Connect the signal to be measured to the required channel A input socket.

CAUTION input must not exceed 50 V r.m.s.

The measured frequency is read directly in Hz, kHz or MHz depending on the setting of the TIME BASE switch.

2.6 PERIOD MEASUREMENT

Functional description

With the FUNCTION switch set to PERIOD A, the instrument measures the period of one cycle of a signal applied to the A channel.

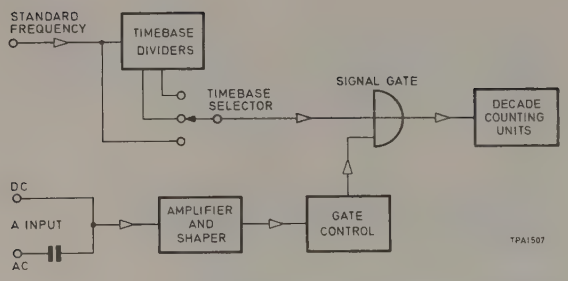


Fig. 2.3 Functional diagram: PERIOD A

Fig. 2.3 shows a simplified functional diagram of the instrument in this operating mode. The signal gate is opened at a point on one cycle of the input signal. This allows pulses, selected by the TIME BASE switch, from the time base or frequency standard to pass through the gate to the decade counting units. The pulses are counted until the gate is closed at the same point on the next cycle of the input signal.

Operating procedure

Set the controls as follows:

FUNCTION switch to PERIOD A.

TIME BASE switch for the desired timing units (note, position 1 is inoperative).

GATE switch to AUTO.

DISPLAY control and MEMORY switch as required.

TRIGGER LEVEL A, FINE control to AUTO TRIGGER. If manual triggering is required, see Sect. 2.4 for details.

Connect the signal to be measured to the required channel A input socket.

CAUTION input must not exceed 50 V r.m.s.

The measured period is read directly in seconds, milliseconds or microseconds depending on the setting of the TIME BASE switch.

2.7 MULTIPLE PERIOD MEASUREMENT

Functional description

With the FUNCTION switch set to MULTIPLE PERIOD A, the instrument measures the period of a signal applied to the A channel. This FUNCTION switch setting gives greater accuracy in period measurement than the PERIOD A position.

Fig. 2.4 shows a simplified functional diagram of the instrument in this operating mode. The signal gate is opened at a point on one cycle of the signal applied to the A channel. When the gate opens a 1 kHz clock signal from the time base or a 10 MHz clock signal from the frequency standard (as selected by the FUNCTION switch) passes through to the decade counting units. The clock signal is counted by the decade counting units until the gate is closed at the same point on a later cycle of the input signal. The SCALING FACTOR switch determines which of the subsequent cycles closes the signal gate.

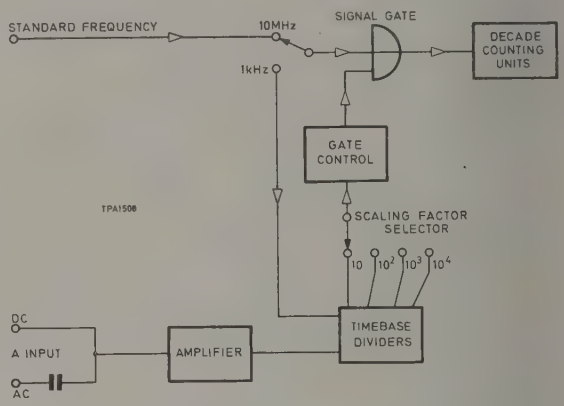


Fig. 2.4 Functional diagram: MULT PER B

Operating procedure

Set the controls as follows:

FUNCTION switch to MULTIPLE PERIOD A, 1 kHz CLOCK or 10 MHz CLOCK as required.

SCALING FACTOR switch to the desired multiplying factor; note that this is limited to 10^4 when using 1 kHz clock.

GATE switch to AUTO.

DISPLAY control and MEMORY switch as required.

TRIGGER LEVEL A, FINE control to AUTO TRIGGER.

If manual triggering is required, see Sect. 2.4 for details.

Connect the signal to be measured to the required channel A input socket.

CAUTION input must not exceed 50 V r.m.s.

The readout will be in ms (for 1 kHz timing units) or μs (for 10 MHz timing units) and should be divided by the factor selected on the SCALING FACTOR switch.

2.8 SCALING

Functional description

With the FUNCTION switch set to SCALE A, the instrument divides the input to the A channel by a selected factor, and totalizes the result.

Fig. 2.5 shows a simplified functional diagram of the instrument in this operating mode. The time base dividers divide the number of cycles of the A channel input by a selected factor, and routes them through the signal gate to the decade counting units. The decade counting units count the scaled-down number of cycles while the gate is open. The signal gate is opened and closed manually.

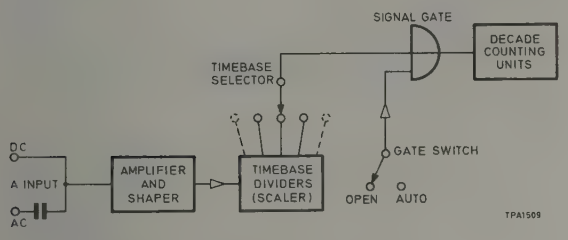


Fig. 2.5 Functional Diagram: SCALE A

Operating procedure

Set the controls as follows:

FUNCTION switch to SCALE A.

SCALING FACTOR switch to the desired multiplying factor.

GATE switch to AUTO.

DISPLAY control to ∞.

TRIGGER LEVEL A, FINE control to AUTO TRIGGER. If manual triggering is required see Sect. 2.4 for details.

Connect the signal to be counted to the required channel A input socket.

CAUTION input must not exceed 50 V r.m.s.

To start counting, set the GATE switch to OPEN.

To stop counting, return the GATE switch to AUTO.

On completion of the measurement, press the RESET switch to erase the readout. The results of two or more measurements may be added by not operating the RESET switch at the end of each measurement.

To obtain the correct pulse count, multiply the readout by the factor originally selected.

2.9 TOTALIZING

Functional description

With the FUNCTION switch in the COUNT A position the instrument totalizes the input. Fig. 2.6 shows a simplified functional diagram of the instrument in this operating mode.

The input is connected to one of the A channel sockets and the decade counting units count the total number of cycles which occur while the signal gate is open. The gate is opened and closed manually.

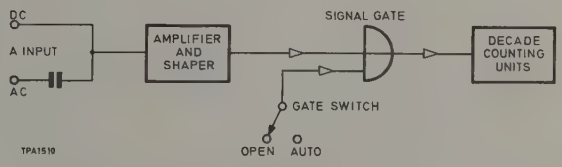


Fig. 2.6 Functional diagram: COUNT A

Operating procedure

Set the controls as follows:

FUNCTION switch to COUNT A.

GATE switch to AUTO.

DISPLAY control to ∞.

TRIGGER LEVEL A, FINE control to AUTO TRIGGER. If manual triggering is required see Sect. 2.4 for details.

Connect the signal to be counted to the required channel A input socket.

CAUTION input must not exceed 50 V r.m.s.

To start counting set the GATE switch to OPEN.

To stop counting return the GATE switch to AUTO.

On completion of the measurement, press the RESET switch to erase the readout. The results of two or more measurements may be added by not operating the RESET switch at the end of each measurement.

2.10 TIME INTERVAL MEASUREMENT

Functional description

With the FUNCTION switch set to TIME B-C, the instrument measures the time interval between a pulse applied to the B channel input and another pulse applied to the C channel input.

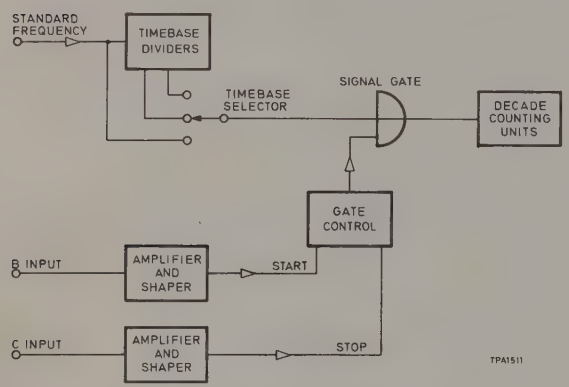


Fig. 2.7 Functional diagram: B—C

Fig. 2.7 shows a simplified functional diagram of the instrument in this operating mode. Pulses selected by the TIME BASE switch are obtained from the frequency standard or time base dividers and applied to one input of the signal gate. When the start pulse from the B input is applied to the other input of the gate, these pulses are passed to the decade counting units where they are counted until the stop pulse applied to the C input closes the gate.

Operating procedure

Set the controls as follows:

FUNCTION switch to TIME B-C.

TIME BASE switch for the desired timing units (note that position 1 is inoperative; i.e. there are no 10 s timing units).

GATE switch to AUTO.

DISPLAY control as required.

Connect the start signal to the B channel input and the stop signal to the C channel input.

CAUTION inputs must not exceed 10 V peak.

The measured time interval is read directly in seconds, milliseconds or microseconds depending on the setting of the TIME BASE switch.

2.11 MEASUREMENT OF EVENTS DURING A SELECTED TIME INTERVAL

Functional description

With the FUNCTION switch set to A/B-C the instrument measures the number of events (pulses, etc.) which are applied to the channel A input between the time one signal is applied to the B channel and another signal to the C channel.

This function may also be used to measure the time interval between two signals applied to the B and C channels, using an external standard frequency as the input to the A channel.

Fig. 2.8 shows a simplified functional diagram of the instrument in this operating mode. The 'start' signal is applied to the B channel input: this opens the signal gate and allows pulses derived from the A channel input to pass to the decade counting units. These pulses are counted by the decade counting units until the gate is closed by the 'stop' signal applied to the C channel.

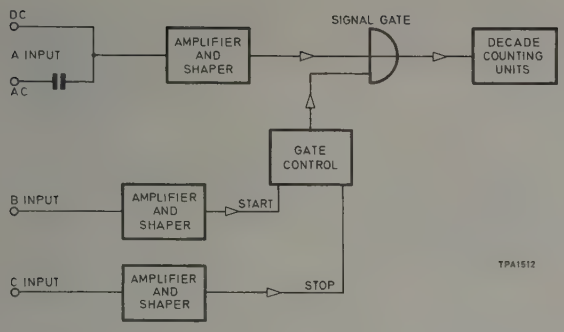


Fig. 2.8 Functional diagram: A/B—C

Operating procedure

Set the controls as follows:

FUNCTION switch to A/B-C.

GATE switch to OPEN.

DISPLAY control as required.

TRIGGER LEVEL A, FINE control to AUTO TRIGGER. If manual triggering is required see Sect. 2.4 for details.

Connect the source of events to be counted (or external frequency standard) to the required channel A input socket and ensure that counting occurs.

CAUTION input must not exceed 50 V.

Now set the GATE switch to AUTO.

Connect the start signal to the B channel socket and the stop signal to the C channel socket. The display obtained will be a number of cycles and will have no units.

2.12 MULTIPLE FREQUENCY RATIO MEASUREMENT

This function can be performed if the instrument has a standard frequency plug-in with an external standard facility which is independent of frequency; i.e. TM 9888.

To make a measurement, connect the higher frequency to one of the A channel sockets and the lower frequency to the external standard input socket on the frequency standard plug-in. Switch to external standard, set the controls for FREQ A (see Sect. 2.5) and proceed as for frequency measurement. Remember that the display is the ratio of the two frequencies and is a number, not a frequency.

The input to the external standard socket should, where possible, be a square wave. If a sine wave is all that is available, the frequency should not be above about 10 kHz. This limit can be overcome to some extent by increasing the input level.

Direct ratio measurement is not possible owing to position 9 of the time base switch being inoperative for frequency measurements. This means that the frequency applied to the external standard socket cannot be used without being divided.

2.13 PRESCALER

When using a prescaler to make a frequency measurement, set the controls as follows:

FUNCTION switch to PRESCALER.

TIME BASE as required.

GATE switch to AUTO.

TRIGGER LEVEL A control to AUTO TRIGGER.

DISPLAY control and MEMORY switch as desired.

Connect the output of the prescaler to the a.c. input of the A channel. The display obtained will be a direct reading of the frequency measured.

2.14 CONNECTING A PRINTER

A 50-way Amphenol plug, type 57-30500 must be fitted to any equipment that is to be driven by the counter. This plug will mate with the optional PRINTER socket on the rear panel of the counter.

The PRINTER connector provides binary coded decimal outputs from the decade counting units which can be used to feed a printer on a remote readout. The connector also carries a 'print command' output and 'inhibit' input signals.

Table 2.1 shows the signal carried on each pin of the PRINTER connector. The groups of binary coded outputs and the corresponding digits are listed sequentially from the right-hand end of the seven digits readout.

Table 2.1

Pin number	Output (approx.)	Function
47	Positive pulse, 0 to +2 V, >10 μs wide.	Print command
48	> +2 V. Provided by contact closure in printer.	Inhibit
49	+3.7 V. May be used to provide inhibit.	
50	earth	
1	0 or +3 V representing '0' or '1'	
2	0 or +3 V representing '0' or '2'	1st digit
26	0 or +3 V representing '0' or '4'	(reading from right)
27	0 or +3 V representing '0' or '8'	
3	0 or +3 V representing '0' or '1'	
4	0 or +3 V representing '0' or '2'	2nd digit
28	0 or +3 V representing '0' or '4'	
29	0 or +3 V representing '0' or '8'	
5	0 or +3 V representing '0' or '1'	
6	0 or +3 V representing '0' or '2'	3rd digit
30	0 or +3 V representing '0' or '4'	
31	0 or +3 V representing '0' or '8'	
7	0 or +3 V representing '0' or '1'	
8	0 or +3 V representing '0' or '2'	4th digit
32	0 or +3 V representing '0' or '4'	
33	0 or +3 V representing '0' or '8'	
9	0 or +3 V representing '0' or '1'	
10	0 or +3 V representing '0' or '2'	5th digit
34	0 or +3 V representing '0' or '4'	
35	0 or +3 V representing '0' or '8'	
11	0 or +3 V representing '0' or '1'	
12	0 or +3 V representing '0' or '2'	6th digit
36	0 or +3 V representing '0' or '4'	
37	0 or +3 V representing '0' or '8'	
13	0 or +3 V representing '0' or '1'	
14	0 or +3 V representing '0' or '2'	7th digit
38	0 or +3 V representing '0' or '4'	
39	0 or +3 V representing '0' or '8'	

Chapter 3

Technical description

3.1 OVERALL SYSTEM

Fig. 3.1 shows a simplified block diagram of TF 2411.

The input signal is a.c. or d.c. coupled to the A channel amplifier. From there it is routed through the main counter gate to the decade counting units where it is counted, and the result is passed to the readout tubes to be displayed.

The open or shut condition of the main gate is determined by either the manual gate switch or the gate bistable on the logic board. A display hold signal ensures that the main gate is held shut during the selected display time. At the end of the display time the decade counting units are reset and, after a short delay which ensures completion of the resetting, the counting cycle is repeated on the next start pulse.

Time base frequencies are derived from a frequency standard plugged in at the rear of the instrument (a number of standards are available). The standard frequency may be derived in the plug-in unit or from an external source. The standard frequency drives an integrated circuit time base, and the time base frequency or scaling factor is selected by front panel controls.

3.2 LOGIC DEFINITIONS

Fig. 3.2 defines the logic symbols which are used in the block diagrams and circuit diagrams throughout the instrument.

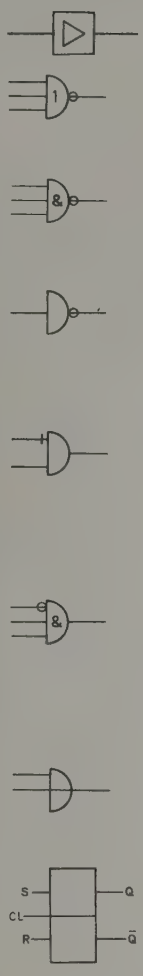

amplifier
1
NOR gate
one or more input in the '1' state gives a '0' state output.
&
NAND gate
all inputs must be in the '1' state to give a '0' state output.
negater
the output is in the '1' state when the input is in the '0' state, and vice versa.
inhibit gate
the inhibit input in the '1' state prevents a '1' state output no matter what the state of the other input (or inputs).
&
AND gate with negated input
the negated input must be in the '0' state and the other inputs in the '1' state to give a '1' state output.
linear gate
the output has the characteristics of the through input.
S
CL
R
Q
Q̄
JK bistable
a trigger input (centre) will set to the '1' state that output whose corresponding input is in the '1' state.

Fig. 3.2 Logic symbols

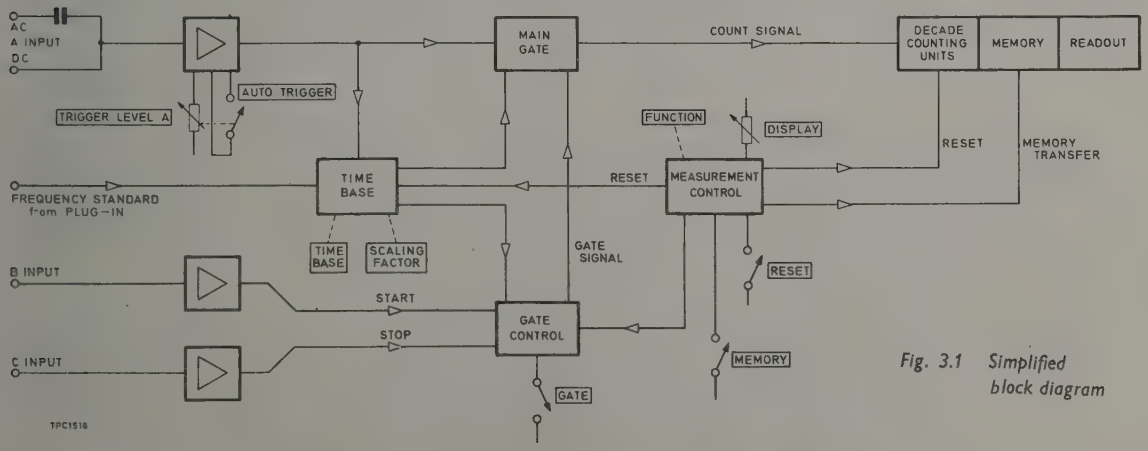


Fig. 3.1 Simplified block diagram

3.3 AMPLIFIER BOARD

(circuit diagram, Fig. 7.2)

This board contains the amplifiers for the three input channels, and a local +11 V power supply.

A Amplifier

The A amplifier consists of a high impedance input stage, a d.c. to 60 MHz amplifier, a Schmitt trigger and an output pulse shaper. Fig. 3.3 shows a simplified block diagram of the amplifier.

Inputs are fed to FET VT5 which has a very high input impedance. This transistor is protected from overloads by diodes MR3 to MR6, the relevant pair of diodes conducting when the input exceeds ±1.4 V with respect to chassis.

The output from VT5 is fed via emitter follower VT6 to one input of differential amplifier VT7/VT8; the other input is derived from the trigger level control circuit and fed in via VT9. Manual triggering is effected by the coarse and fine front panel controls which give a ±1 V d.c. offset to the A input. Automatic triggering is achieved by setting the fine control to the extreme counter-clockwise position which disconnects the manual controls and switches in a feedback amplifier, VT22. This amplifier responds to the mean d.c. voltage at the main amplifier output and holds this output at a level suitable for the Schmitt trigger. As the input to VT22 is via low-pass filter R62/C24, automatic triggering is limited to frequencies above about 1 kHz.

The first differential amplifier drives a similar amplifier, VT10/VT11, and the output from this is fed to the main amplifier, VT12/VT13. H.F. cut control is in the signal line between the differential amplifier and the main amplifier. When control signal L16 is high, VT21 is switched on; this loads the signal line with C26 giving 30 dB attenuation above 10 MHz.

Schmitt trigger VT14/VT15 is of conventional design and is driven by the main amplifier. The output signal from the Schmitt trigger is a.c. coupled to the output pulse shaper where it is differentiated by C19 and R48, and clipped by MR8 to provide a negative pulse to trigger VT16. The output from VT16 is a 50 ns pulse which is passed to the count board to be counted or to be fed through to control the main gate, depending on the function.

B and C Amplifier

These amplifiers are identical. Two transistors form a differential amplifier, the base of the second transistor being earthed. The input is protected against overloads by two diodes (MR11 and MR12 for the B amplifier), and the output is prevented from going negative by another diode (MR13 for the B amplifier). The output must be kept positive to avoid damage to the integrated circuits which follow the B and C amplifier stages.

Power supply

This produces a +11 V line from the unregulated +20 V line.

Zener diode MR1 provides the reference voltage which is fed to the non-inverting input of integrated amplifier IC1; potential divider R1, R2, R3 provides the control input. Emitter followers VT2 and VT3 buffer the amplifier output and supply two +11 V lines which are used in the A amplifier. VT4 and VT1 give protection against overload currents.

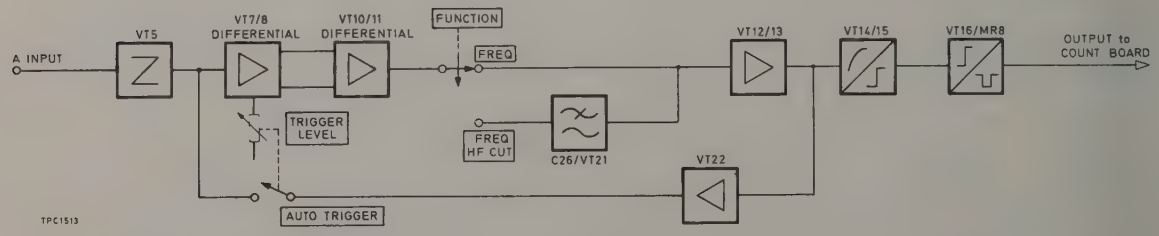


Fig. 3.3 Functional diagram for A amplifier

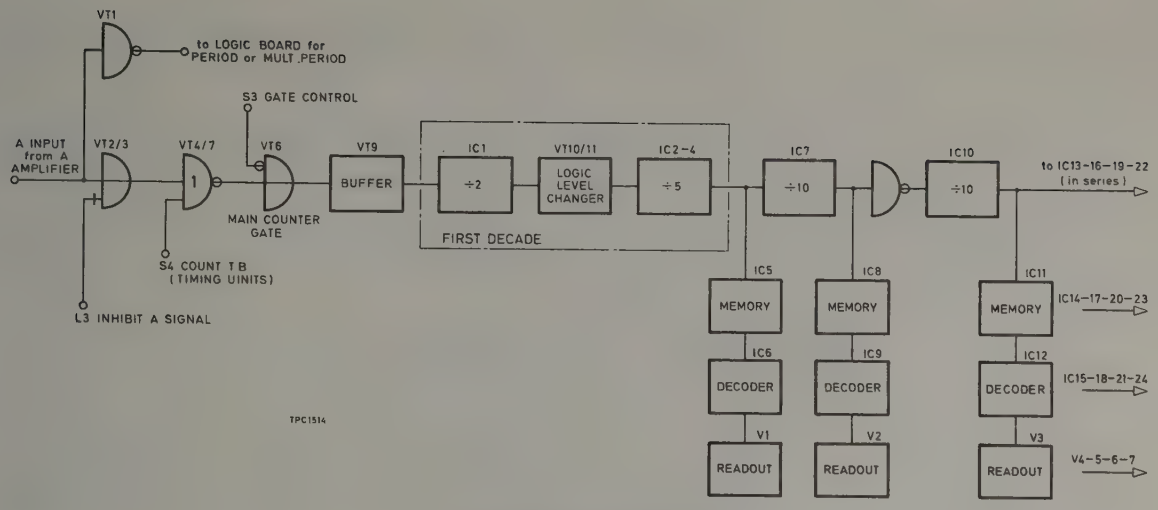


Fig. 3.4 Functional diagram of counting chain

3.4 COUNT BOARD

(Circuit diagram, Fig. 7.3)

This board contains the main counter gate and control gating, decade counting units, memory, readout decoding and display tubes. Fig. 3.4 shows a simplified block diagram of the counting chain.

Input gating

The input A signal from the amplifier board is fed via VT1 to the logic board where it is used to control the main counter gate during period and multiple period measurements.

When used in the counting chain the A signal is fed to VT2, which forms the signal input of an inhibit gate. This gate is controlled, via VT3, by the inhibit A signal (L3) from the logic board, so that the A signal will not pass in functions where timing units are counted.

The output from VT2 is fed to NOR gate VT4/VT7 which passes the A signal or timing units to the main counter gate, VT6. The open/shut condition of VT6 is controlled by the gate bistable on the logic board.

Decade counting units

The output from the main counter gate is buffered in VT9 and fed to the first, high speed, decade.

In the first decade, the divide by ten operation is done in two stages; divide by two in IC1 and divide by 5 in IC2 to IC4. VT10 and VT11 adjust the output level of the binary divider to suit the quinary integrated circuits.

The quinary divider is similar in operation to a discrete component divider; Fig. 3.5 shows the internal gating. The 'K' input gates of IC2 and IC4 are held open by the d.c. supplies. The Q outputs of IC2 and IC3 are combined in an AND gate, of output of which drives the 'J' inputs of IC4. On receipt of the fourth input cycle, IC4 switches into the 'set' state (i.e. the Q output is active); this removes the $\overline{Q}$ signal (on pin 6) from the 'J' input of IC2 thus preventing the fifth input cycle from affecting this integrated circuit. The fifth cycle switches IC4 which leaves the three integrated circuits in the '0' state, ready for the next input.

IC7 is the second decade of the counting chain. The output from this is inverted in VT12 to provide signals of the necessary level and polarity for the subsequent decades (IC10 etc. which use negative logic).

Memory

This consists of seven integrated circuits, one per decade and each containing four bistables.

When the memory is off the bistables accept information from the decades and transfer it to complementary outputs. When the memory is on, the bistables hold the information from one measurements while the next count is taking place, and only accept the new data on receipt of the memory transfer pulse, (S14).

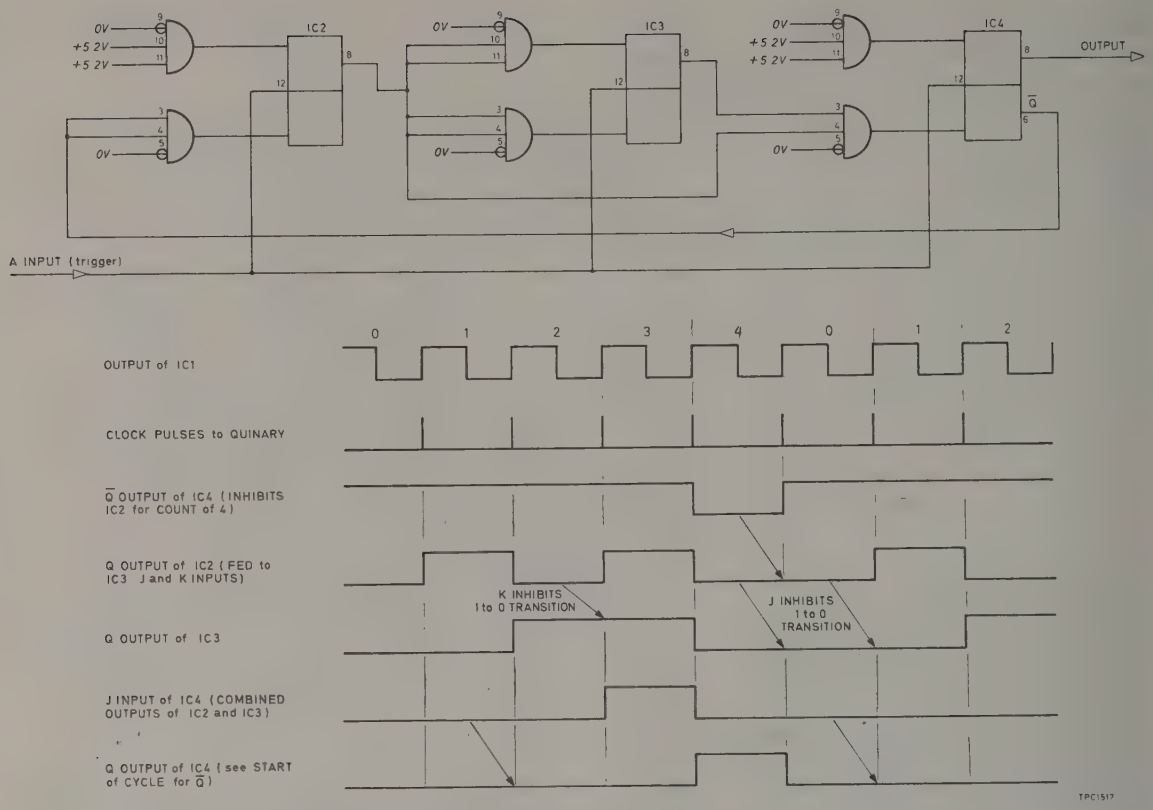

0V
+5 2V
+5 2V
IC2
IC3
IC4
OUTPUT
A INPUT (trigger)
OUTPUT of IC1
CLOCK PULSES to QUINARY
Q̄ OUTPUT of IC4 (INHIBITS IC2 for COUNT of 4)
Q OUTPUT of IC2 (FED to IC3 J and K INPUTS)
Q OUTPUT of IC3
J INPUT of IC4 (COMBINED OUTPUTS of IC2 and IC3)
Q OUTPUT of IC4 (see START of CYCLE for Q̄)
K INHIBITS 1 to 0 TRANSITION
J INHIBITS 1 to 0 TRANSITION
0 1 2 3 4 0 1 2
TPC1517

Fig. 3.5 Functional diagram of the quinary divider showing internal gating and timing. Arrows indicate where transition (0 to 1 or 1 to 0) is inhibited from taking place by presence of '0' state

Readout

B.C.D. to decimal decoding, and driving of the display tubes take place in one integrated circuit for each decade. The integrated circuit accepts negative logic b.c.d. from the memory, decodes it, and switches one of ten high voltage outputs. This earths one of the readout tube cathodes, forcing the relevant digit to strike. The ten output wires from the integrated circuit are taken to the tube by means of flexible printed wiring attached to the count board by an edge connector.

Reset

The reset input signal (S15) is a positive pulse which is used to reset to zero all decades except the fastest.

A negative pulse for resetting the three integrated circuits in the quinary divider is obtained by inverting the reset input (S15) in VT5. The short, positive pulse required for resetting IC1 is obtained by differentiating the output of VT5 in C5, R16 and R17, and inverting the resultant signal in VT8.

Although resetting of the quinary integrated circuits is asynchronous, it will occur only when the clock input is low. If the output from IC1 is high the clock must be forced low before resetting can occur. This is done by applying the positive spike from VT8 to the collector of VT10 which turns on VT11 for the necessary resetting time. Since IC1 is reset at the same time, removal of the pulse after a short delay will not cause a count to occur.

3.5 LOGIC BOARD

(Circuit diagram, Fig. 7.4)

This board contains the time base dividers, main counter gate control logic, display control, reset monostable and the gating necessary to produce the programming signals required to condition the instrument for any particular function. Fig. 3.6 shows a simplified block diagram of the board.

Programming signals

The function switch and the gates in IC1 to IC4 produce programming signals (labelled L)

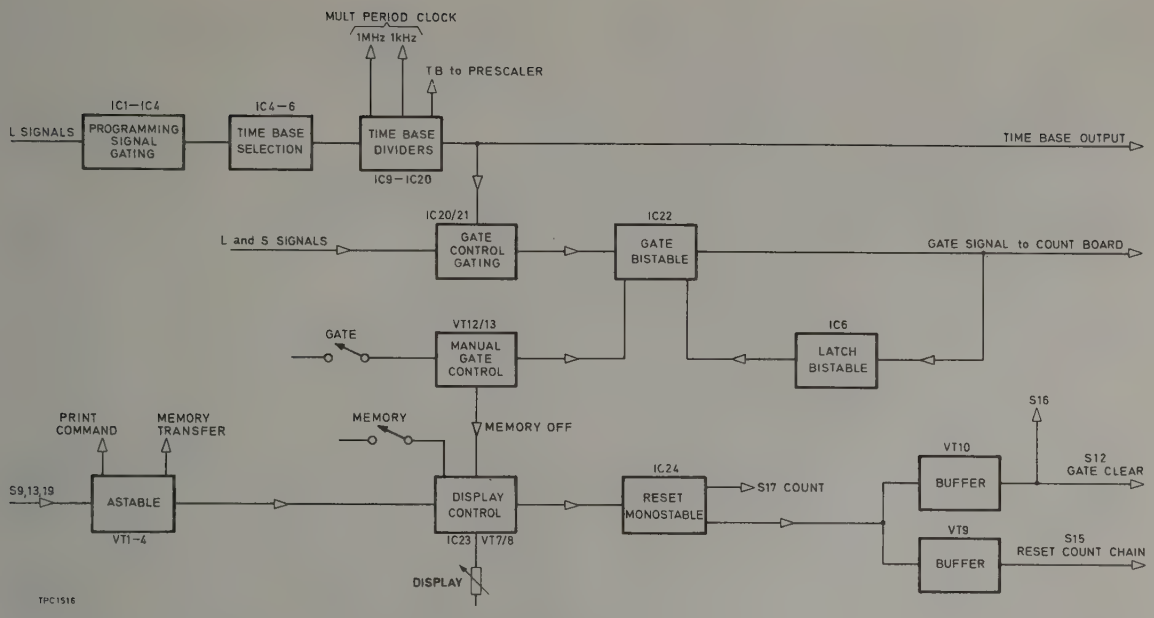


Fig. 3.6 Logic board functional diagram

which are used to condition the instrument for any given function. The integrated circuit gates simply invert or combined the function switch d.c. levels to give the necessary signal.

Time base

The time base comprises eight integrated decade dividers; gating in IC4b and IC5 determines which signal drives the dividers.

When using a prescaler, the prescaler select signal (L15) prevents the output of the first divider (IC7) from driving subsequent dividers; S6, the prescaler time base, is substituted as the drive at this point. The time base is also controlled after divider IC12 to allow the 1 kHz time base to be brought out for multiple period measurements with 1 kHz clock.

A time base output from each divider is fed to a NAND gate where it is available for selection by the appropriate time base select signal, T1 to T9. The output from each of these NAND gates is connected in a distributed OR function and fed via NAND gate IC19c and NOR gate IC19d to the count board as S4, count time base signal; S4 is counted in period, time and scaling measurements. The 10 MHz signal for use in multiple period measurement is also fed, via IC20b, through IC19d to the count board.

The time base dividers are reset to 0 or to 9 depending on the function being performed. This resetting is effected by feeding the reset time base signal, S16, to the 'reset to 0' and 'reset to 9' inputs of each divider and gating it with the appropriate function select signal.

Gate Control

The open/shut condition of the main counter gate is determined by S3 which is fed to the count board via NOR gate IC3b. L7 conditions the gate for period, multiple period (10 MHz clock), scaling and time measurement, while the gate bistable, IC22, provides the control signal for all other functions. Gates in integrated circuits IC20 and IC21 determine which function triggers the gate bistable.

In the reset state the Q outputs of the gate bistable (IC22 pin 8) is at '0' and the latch bistable output (S13) is at '1'.

On receipt of a trigger pulse (start) the gate bistable switches and produces a signal to open the main counter gate. This trigger pulse also switches the latch bistable, IC6b and IC6c, which sets S13 to the '0' state.

The next trigger pulse (stop) switches the gate bistable Q output to '0' but has no effect on the latch bistable since the cross coupling provides one '0' input to IC6c. As S13 from the latch bistable remains at '0' further trigger pulses have no effect on the gate bistable.

At the end of the display time the reset pulse, S12, goes to '0' resetting the latch bistable, leaving it ready for the next trigger pulse.

For manual gate operation a d.c. level from the gate switch is fed via VT12 and VT13 to the gate bistable, holding it in the reset state.

Display and memory

Display control circuit VT7/VT8 is essentially an inhibited free running oscillator. On triggering, VT6 switches off which permits C4 to charge. VT8 emitter follows and the emitter of VT7 rises until the unijunction eventually triggers. This discharges C4 through MR9, VT7 and R34 returning the circuit to the stable state. During the discharging of C4 the negative pulse on base 2 of VT7 resets the cross coupled gate bistable, IC23b and IC23c. via C3.

The display circuit is initially triggered by astable VT3/VT4 which is included as a safeguard against the instrument attaining a stable state (due to abnormal gate control conditions) and being non-operable on switch-on. This astable produces a pulse which is greater than 10 μs wide but it is normally inhibited by transistors VT1 and VT2.

The astable also provides a print command pulse (S18), and a memory transfer pulse (S14) which is fed via inhibit gate IC23a to buffer transistor VT5. This memory transfer pulse is inhibited by the output from VT12 when manual gate control is selected.

An inhibit is imposed on the display and memory circuits when a signal is applied to an input of OR gate MR1 to MR3. This inhibit is fed via MR7 to the display bistable, and is also applied to the astable to prevent a memory transfer pulse from being produced.

Reset

At the start of the display cycle a display trigger pulse via VT6 will appear as a positive spike at the input of the reset monostable (owing to C5) but will not affect it. At the end of the display cycle VT6 turns on, triggering the reset monostable which produces a nominal 100 μs pulse. This pulse is differentiated at the input of buffers VT9 and VT10 and passed through to reset the various circuits throughout the instrument. During the reset time S17 is in the '0' state and this inhibits the gate bistable, preventing a count until resetting is complete.

3.6 POWER SUPPLY

(Circuit diagram, Fig. 7.5)

MR8 and MR11 form a full wave rectifier which produces the +20 V line for use in the amplifiers and frequency standard.

The +20 V line is also smoothed and regulated by VT1 to about 11.5 V; MR14 further smooths and regulates this to 7.5 V and this voltage is then used as the reference for the main supply lines.

VT2 and VT3 form a differential pair which compares the +5.2 V supply with the part of the reference voltage derived from potential divider R5, R6 and R7. The output from VT3 is passed via amplifier VT5 to drive the series regulator VT8.

+4.5 V and +3.7 V supplies are derived from the +5.2 V line by MR17 and MR15; these lines are used for the DTL and the RTL integrated circuits, respectively.

The +8 V line is used to produce the +5.2 V line and is obtained from bridge rectifier MR5, 6, 9 and 10. This produces an unstabilized line, C1 being used as the reservoir capacitor.

The +5.2 V, +4.5 V and +3.7 V lines have overload protection which prevents their combined currents from exceeding 2 A. As the combined current rises, the voltage developed across R14 rises to 0.7 V at which point VT6 conducts. This turns on VT4 which has the effect of reducing the output voltage.

In the event of a short circuit developing in the regulator transistor, VT8, Zener diode, MR16, limits the output voltage to about +5.9 V.

The readout tube supply is obtained from the voltage doubler circuit, MR3, MR4 and capacitors C5-7 and C8-10 (which form the two equivalent capacitors).

A -3.5 V supply, for use in the B and C amplifiers, is generated by diodes MR1 and MR7. These provide about -20 V which is then regulated by MR2 and R2 to the required voltage.

3.7 FREQUENCY STANDARDS

(circuit diagram: Fig. 7.6)

10 MHz standard: TM 9888

Crystal XL1 drives the single stage oscillator, VT1, C1 giving fine adjustment of the frequency.

The output of VT1 is a.c. coupled via C7 to the output transistor VT3. VT3 is base biased to ensure that it is off when there is no input signal present; this prevents noise breakthrough to the counter circuits.

When an external standard is being used, the signal is a.c. coupled via a diode protection circuit (MR2 and MR3) into VT2. The output of VT2 is fed, as for internally generated signals, to VT3.

VT1 and VT2 act as an OR gate which passes either the internal or external standard as required; switch SA connects the base of the unused transistor to earth.

External frequency standard: TM 9890

This unit is essentially a 10 MHz multiplier which acts any sub-harmonic of 10 MHz above 833 kHz.

The external standard is fed via diode protection network, MR1 and MR2, to VT1. The output of this transistor is squared in Schmitt trigger VT2 and VT3 and the output amplified in VT4. Tuned circuit L1 and C5 multiply the output of VT4 to 10 MHz and this is passed via the two amplifier stages, to the counter.

Internal frequency standard: TM 9933

The standard frequency is generated by an oven controlled crystal oscillator. The oven uses a +12.6 V supply which is derived from the +20 V line by differential amplifier, VT3 and VT4, using the +5.2 V line as the reference.

External adjustments of the standard frequency are made by RV1 which is connected to a varactor fine frequency control within the oven.

The oscillator output is isolated from earth and has a high stability load (R1) for optimum performance. The output is fed via the high impedance emitter follower, VT1, to the output amplifier, VT2.

Chapter 4

Maintenance

4.1 INTRODUCTION

This chapter of the manual is intended as a guide to keeping the instrument in good working order; instructions are also given for checking the overall performance of the instrument.

The only part of the instrument which may need regular attention is the internal standard oscillator, where the frequency standard plug-in has one. This should periodically be adjusted to compensate for any drift which has taken place (see Sect. 4.7). Other preset components should not need adjustment unless associated components are replaced.

Integrated circuits and semiconductor devices are used throughout the instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reversed polarity and excessive heat or radiation. Avoid hazards such as prolonged soldering, strong r.f. fields or other forms of radiation, the use of insulation testers, and accidentally applied short circuits.

When removing integrated circuits a special soldering iron should be used as all leads must be unsoldered together to release the device.

4.2 FUSES

The counter is protected by a delay fuse (FS1) in the line conductor of the mains supply. This fuse is 500 mA for 240 V and 1 A for 115 V supplies. The fuse holder is screw cap and is located on the rear panel.

FS2 is a 2 A delay fuse in the +8 V line, protecting the +5.2 V line from prolonged overloads. This fuse is mounted on the power supply board and the top cover must be removed before it can be replaced.

4.3 ACCESS TO COMPONENTS

Access is gained to most components on removal of the instrument covers. The count and logic boards can be hinged on their sockets to make available all other components or wiring (see below). Figs. 4.1, 4.2 and 4.3 show views of the instrument with covers removed.

Power supply and amplifier printed wiring is made available only on removal of the relevant board. Each board is held to the chassis by four screws.

Removing covers

The top and bottom covers fit into a groove in the front panel trim, and each is held by two screws in the rear panel. Removal of the screws releases the covers which can then be removed.

Count board

Removal of the top cover gives access to the components on the Count board. This board can be hinged to the side to expose its printed wiring, components on the frequency standard unit, etc. (see Fig. 4.1). To release the board, slacken the two screws at the side of the instrument (see Fig. 4.2) and remove the screw which clamps the board to the chassis (see Fig. 4.1). The board and display assembly can now be pushed back about 5 mm (in the horizontal plane) to clear the locating pin, and then hinged upwards, to the side.

Logic board

The logic board can similarly be hinged clear to give access to components on the board and to the mains transformer tappings. Remove the three screws which secure the board (see Fig. 4.3) and then hinge it to the side.

Frequency standard unit

The frequency standard unit is plugged in at the rear panel, and secured by one screw. Removal of this screw (see Fig. 4.1) allows the unit to be withdrawn.

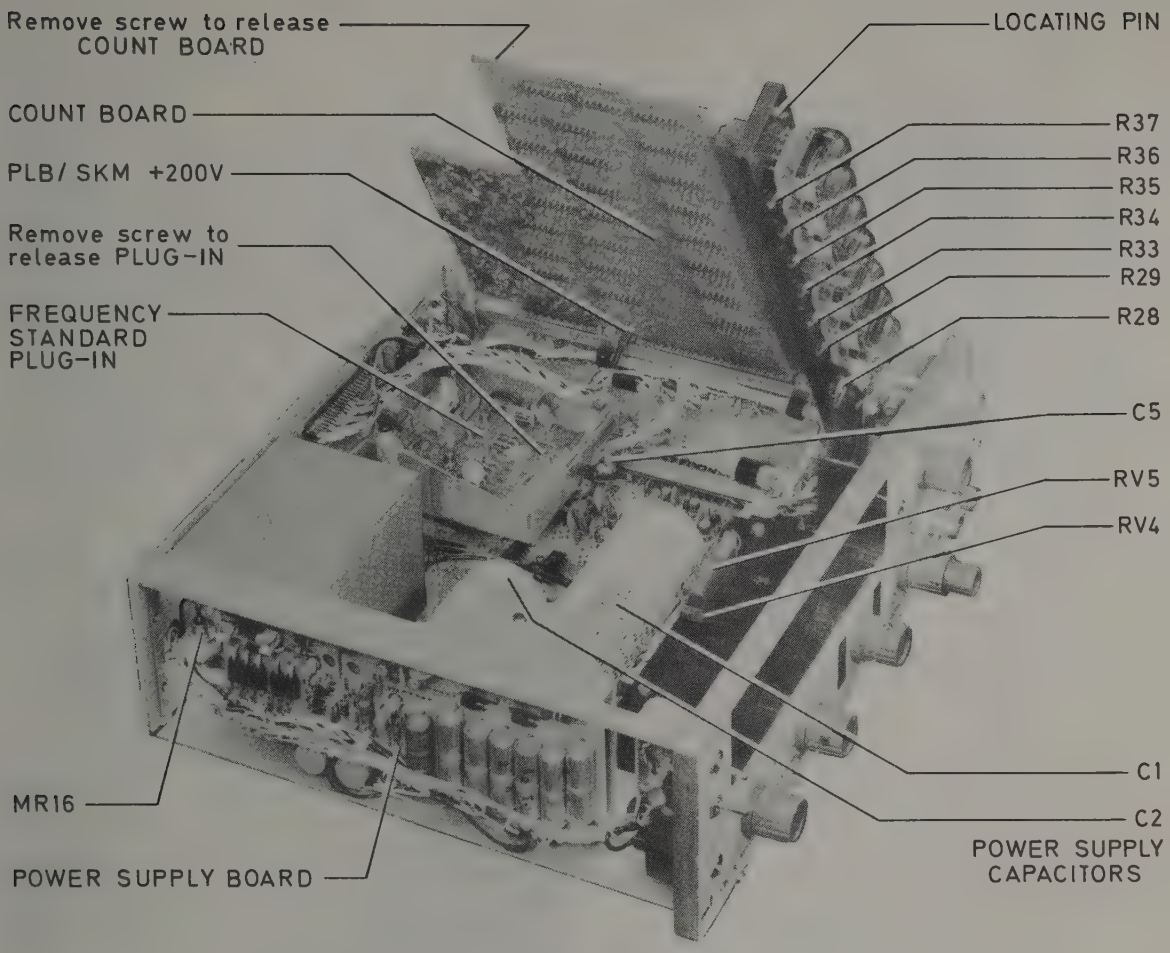


Fig. 4.1 Internal view of instrument looking into top

4.4 SUPPLY VOLTAGE— TRANSFORMER CONNECTIONS

The counter can be adjusted to operate from any supply in the range 100 V to 130 V and 200 V to 250 V, 45 to 60 Hz. For this purpose it is fitted with a mains transformer which has two tapped primary windings (see circuit diagram, Fig. 7.5). For the higher voltage range the two primaries are linked in series; for the lower range they are linked in parallel. When the primaries are linked the supply is connected to taps according to the supply voltage.

Connections to the transformer are made at tags on the transformer case (see Fig. 4.3 for location). When the tappings require changing, remove the bottom cover of the instrument and hinge back the logic board (see Sect. 4.3 for details). For the higher voltage range connect TAP A to TAP B; for the lower range connect TAP B to 0 V and TAP A to 100/200 V. Apply the mains input to the tags whose voltage markings sum to the supply voltage. Only the markings appropriate to the linking of the primaries should be added; e.g. for 230 V connect the supply between tags marked +10 V and 120/220 V.

4.5 PERFORMANCE CHECKS

This section outlines tests which check that the counter is operating within its specification. The time base and decade counting units are checked by using the TEST function (see Sect. 2.3, Self Check). The tests should be carried out with a correctly working frequency standard plugged into the instrument.

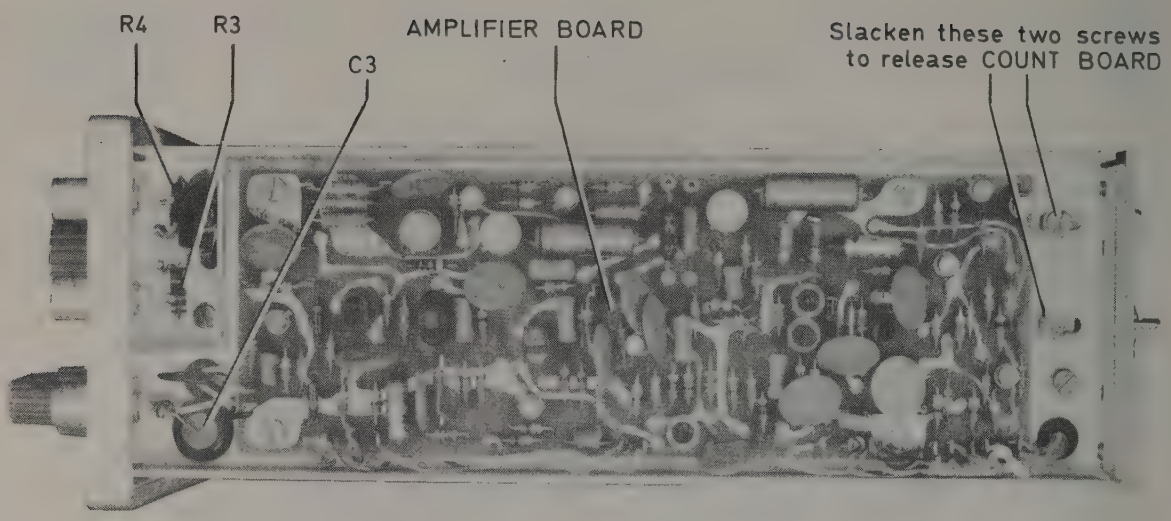


Fig. 4.2 Internal view of TF 2411

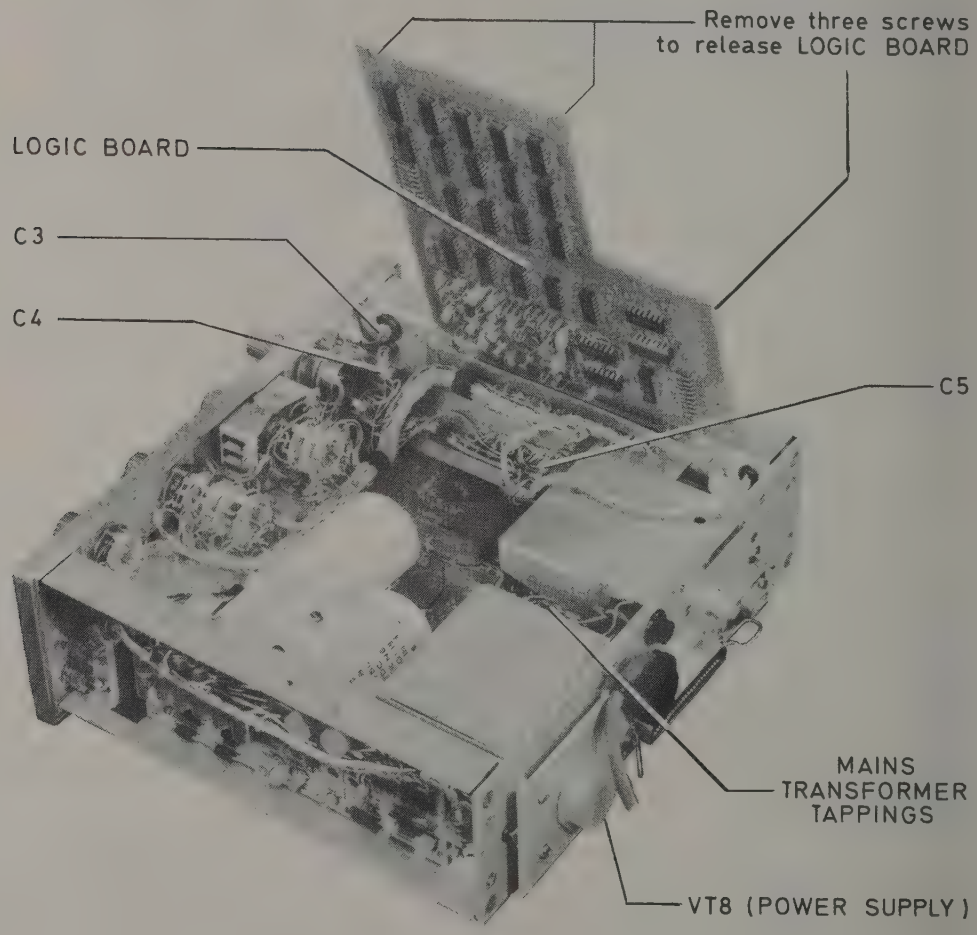


Fig. 4.3 Internal view of TF 2411 looking into bottom of instrument

Table 4.1

Function	Indication	Time base positions								
		1	2	3	4	5	6	7	8	9
TEST FREQ A EXTERNAL PRE-SCALER	decimal point (read from right) units	1 Hz	3 kHz	2 kHz	1 kHz	3 MHz	2 MHz	1 MHz	0 MHz	- -
PERIOD A TIME B-C	decimal point units	- 	0 sec	1 sec	2 sec	0 ms	1 ms	2 ms	0 μs	1 μs
MULTIPLE PERIOD A 1 kHz clock	decimal point units	3 sec	(all time base positions) (all time base positions)							
MULTIPLE PERIOD A 10 MHz clock	decimal point units	4 ms	(all time base positions) (all time base positions)							
SCALE A COUNT A $\frac{A}{B\text{-}C}$		No units displayed								

4.5.1 Test equipment

a) Oscilloscope with x10 probe; 50 MHz bandwidth, e.g. M.I. TF 2210.

b) R.F. millivoltmeter, e.g. M.I. TF 2603.

c) Signal generator; 50 MHz, e.g. M.I. TF 144H.

d) Sensitivity valve voltmeter, e.g. M.I. TF 2600.

e) R-C oscillator, e.g. M.I. TF 1101.

f) T connector, TM 7948 (optional accessory for TF 2603).

g) T connector with B.N.C. sockets.

h) 50 Ω load, TM 7967 (optional accessory for TF 2603).

i) Pulse generator, 200 ns pulse, e.g. M.I. TF 2010.

4.5.2 Decimal points and units

Switch through all positions of the TIME BASE switch for each function, and check that the decimal points and units are displayed as shown in Table 4.1.

4.5.3 Sensitivity (A channel)

Test equipment: b, c, f, g, h.

Connect the test equipment as shown in Fig. 4.4 and set the controls as follows:

Signal generator (TF 144H):	Function	- CW
	Frequency	- 100 kHz
	Output level	- 2 V
Voltmeter (TF 2603):	Range	- 1 V
TF 2411:	Function	- FREQ A
	Time base	- position 3
	Gate	- AUTO
	Memory	- ON
	Display time	- minimum

Adjust the trigger level controls for a correct count of the input frequency.

Reduce the input level and, at the same time, adjust the trigger level, until the minimum input which gives a consistent count is found. This input should not exceed 10 mV.

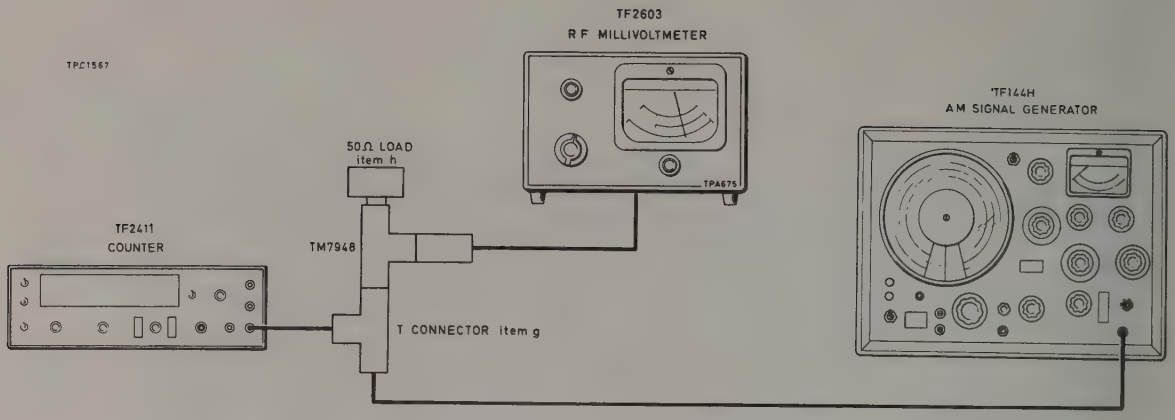


Fig. 4.4 Test gear layout for sensitivity, h.f. cut and auto trigger sensitivity testing

NOTE: See Sect. 2.4 for details of manual triggering at low input levels.

Repeat the above test at a number of frequencies between 100 kHz and 50 MHz. In each case the minimum input should not exceed 10 mV.

4.5.4 H.F. cut

Test equipment: b, c, f, g, h.

Connect the test equipment as in Fig. 4.4 and set the controls as for the previous test (Sect. 4.5.3) but with the signal generator set to 10 MHz.

Determine the sensitivity of the instrument at this frequency as described in Sect. 4.5.3.

Switch the counter to FREQ A, H.F. CUT and repeat the test. The sensitivity should be more than 20 dB down on the original result.

4.5.5 Auto trigger sensitivity

Test equipment: b, c, f, g, h.

Connect the test equipment as in Fig. 4.4 and set the controls as for Sect. 4.5.3, but with the counter TRIGGER LEVEL A, FINE control set to AUTO TRIGGER.

Check that the minimum level required to obtain a consistent readout is not greater than 20 mV at a number of input frequencies between 100 kHz and 50 MHz.

Transfer the input from the d.c. socket to the a.c. socket of the A channel, and with an input of 50 MHz check that the sensitivity is better than 20 mV.

4.5.6 Trigger level error

Test equipment: d, e, g.

Connect the test equipment as shown in Fig. 4.5 and set the controls as follows:

TF 2411:

Function	-	PERIOD A
Time base	-	position 7
Gate	-	AUTO
Memory	-	OFF
Display time	-	about 1/3 clockwise
Trigger level	-	mid-travel

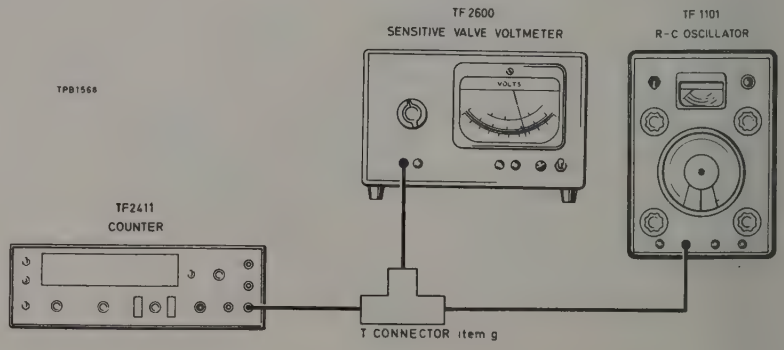


Fig. 4.5 Test gear layout for checking trigger level error

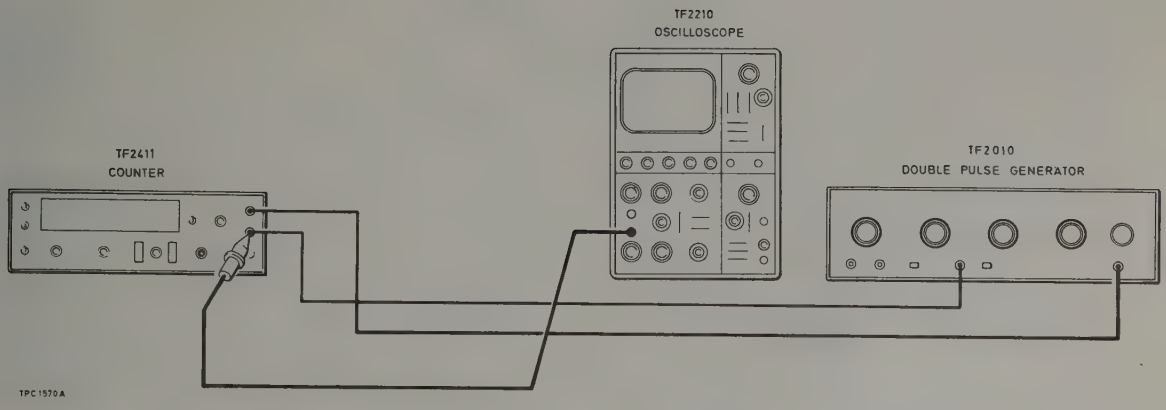


Fig. 4.6 Test gear layout for checking sensitivity of B and C channels

Oscillator (TF 1101): Frequency - 100 Hz

Voltmeter (TF 2600): Range - 100 mV

Adjust the oscillator output level to 100 mV as monitored on the voltmeter.

Set the counter TRIGGER LEVEL controls for the most stable count obtainable, and note the highest and lowest readings displayed on the counter. The difference between the readings should not exceed 6 counts.

Now adjust the oscillator output level to 10 mV, as monitoed on the voltmeter, and repeat the test. The trigger level error should not exceed 60 counts. Adjust the TRIGGER LEVEL FINE control, if necessary, during the test.

4.5.7 Sensitivity (B and C channels)

Test equipment: a, f, g, h, i.

Connect the test equipment as shown in Fig. 4.6, with the oscilloscope probe connected to the B input socket.

Set the controls as follows:

TF 2411:

Function	- TIME B-C
Time base	- position 8
Memory	- off
Gate	- AUTO
Display time	- mid-travel

Oscilloscope:

Input	- 100 mV/cm d.c.
Time base	- 50 ns/cm
Trigger	- internal/auto

Pulse generator:

Function	- single pulse
P.R.R.	- 10 kHz
Pulse width	- 200 ns } Main pulse
Pulse polarity	- positive } and pre-pulse
Delay	- 10 μs

Connect the pre-pulse to the B channel and the main pulse to the C channel. Adjust the pulse generator controls to obtain a 10 μs main pulse 200 ns wide and 400 mV amplitude.

Check that the counter correctly measures the delay between the two pulses (10 μs).

Reduce the pulse amplitude until the minimum level which gives a correct count is found. This should not exceed 300 mV.

Now connect the main pulse to the B channel and the pre-pulse to the C channel and repeat the test. The counter reading should be 90 μs in this case.

4.6 REPLACEMENT OF READOUT TUBES

With normal operation of the instrument, readout tubes should have a life of several years.

When a tube needs replacing, remove the top cover of the instrument and hinge back the count board (see Sect. 4.3). This allows access to the tubes which can then be unplugged.

Replacement readout tubes are B5991, ZM1162 and CD43.

4.7 ADJUSTING THE INTERNAL FREQUENCY STANDARD

The accuracy of the gate times and timing signals is determined by the standard frequency. Before checking the internal standard, the instrument should be thoroughly warmed up.

TM 9888

Remove the bottom cover of the instrument. This allows access for adjustment via holes in the logic board and the cover for the plug-in.

With the FREQ A function selected, set the TIME BASE switch to position 1 (i.e. 10 second gate). Apply a 10 MHz standard frequency to the A channel d.c. input at a level sufficient to trigger the counter. Adjust the oscillator so that the counter reads 000000.0.

This procedure sets up the counter to the same accuracy as the applied standard frequency with an additional possible error of ±1 part in 10^8 (i.e. ±1 count when counting 10 MHz over 10 seconds). This error is increased to ±1 part in 10^7 if a 1 MHz standard frequency is all that is available.

TM 9933

Normally, correction of drift can be made as described above, but in this case adjusting the potentiometer through the hole at the left-hand side of the panel of the plug in. Adjustment of the oscillator itself should rarely be necessary, but in the event of lack of adjustment travel in the normal potentiometer (owing to component replace- shown below. The instrument should be warmed up for at least four hours if optimum adjustment accuracy is required.

Set the instrument to measure multiple period, with 10 MHz clock and a scaling factor of 10^7.

Connect the 10 MHz standard to the A channel d.c. socket. (If a 1 MHz standard is used select a scaling factor of 10^6.)

On TM 9933, set the potentiometer to mid-travel (i.e. 14 turns from the end stop).

Unscrew the white plastic trimming tool from the panel, and remove the black rubber stopper.

Use the trimming tool to adjust the oscillator, (through the hole previously stoppered) until the readout just passes through the nominal frequency (i.e. until the display passes through being all nines or all zeros).

CAUTION To prevent damage to the iron dust core in the oscillator, the trimming tool supplied must be used to make the adjustment, and once the nominal frequency has been passed do not readjust the coarse control.

Complete the adjustment with the normal control, adjusting for a reading of all nines.

Chapter 5

Repair

5.1 INTRODUCTION

This chapter of the manual includes information on fault finding and realignment. It should be used in conjunction with the circuit diagrams in Chap. 7 and the descriptions in Chap.3.

Limits given in this chapter are for guidance only and are not guaranteed specifications unless they are quoted in Sect. 1.2, Data Summary.

For precautions to be taken with the integrated circuits and semiconductors in the instrument, see Sect. 4.1.

In case of difficulties which cannot be resolved with the aid of this book, please contact our Service Division at the address on the rear cover or your nearest Marconi Instruments representative. Always mention the type and serial number of your instrument.

5.2 SUPPLY VOLTAGE LEVELS

The supply lines for each board should be as shown in Table 5.1 below, when measured with a 20 kΩ/V multimeter. Adjustments to the voltages can be made as described in the recalibration procedure (Sect. 5.4).

In addition, on the A amplifier board there are two +11 V (±0.1 V) lines which can be monitored at the positive ends of C6 and C11.

Also, if TM 9933 is used, check that the oven supply is 12.6 V ±5% on pin 5 of the frequency standard board.

5.3 FAULT FINDING

The nature of a fault will often be apparent from its symptom (for example, a faulty readout tube or a gross error on the display time will quickly be seen) and in general faults concerning decades, memory or readout will show in the display Where the cause of a fault is not apparent the following tests, while not exhaustive, will indicate the area in which it is most likely to be found.

Before proceeding with fault finding check that all supply lines are at their correct levels (see Sect. 5.2); a low voltage line can cause errors without making the instrument inoperative.

The checks should be done in the order given in the following chart; vary only those controls mentioned, leave the others as they are set. In general, when monitoring levels, high is more than 1.5 V and low is less than 0.5 V.

Table 5.1

Supply line	Voltage limits	PIN NUMBERS: Power supply board	Count board	Logic board	A amplifier	Frequency standard
+200 V	190 V minimum	15	8	-	-	-
+20 V	18 V minimum	6	-	12	15	1
+5.2 V	±0.1 V	1	F	D & 1	9	4
+4.5 V	4.3 V to 4.6 V	2	-	18	-	-
+3.7 V	3.5 V to 3.8 V	5	H	N	-	-
-3.5 V	-3.0 V to -3.8 V	12	-	-	8	-

FAULT FINDING CHART

Test number	Test conditions	Result	Next test	Area of fault
1	Function : Period Gate : Open Memory : Off Switch through all T.B. positions	a) normal working b) no counting c) counting fails on some T.B. positions d) display incomplete e) 1st decade counts 0, 1, 0, 1 etc.; other decades remain at 0	4 2 3 → →	 Faulty decade or tube Permanent reset present
2	Connect an oscilloscope to the following positions: a) Freq. standard output b) Gate output c) First d.c.u. output	a) b) c) x x x ✓ x x ✓ ✓ x ✓ ✓ ✓ x = signal not present ✓ = signal present	 → → → →	 No standard frequency Gate shut First binary in count chain Memory
3	Connect oscilloscope to T.B. dividers in turn	a) all counting b) some counting	→ →	Select signals T1 to T9 T.B. decades
4	Function : Test Gate : Auto Display : ∞ T.B. : 2 Press reset switch	a) normal working b) continuous counting c) reset incomplete d) no counting	5 → → →	 Gate Reset Gate bistable
5	As test 4 but with display variable	a) counter cycles b) counter doesn't cycle c) some display times fail d) counter cycles once only	6 → → →	 Display control * Display control Astable
6	Memory : On Display : ∞ T.B. : 4 Press reset switch	a) Counter cycles b) Counter doesn't cycle	7 →	 Memory transfer gating
7	Connect a signal to A input and check that the signal appears at the output of the amplifier board (pin 10)	a) signal present b) signal not present	→ →	Programming (S and L) signals for function on which fault first appeared A channel

NOTES: Test 7 should be done on channels B and C if the fault first appeared on a function using either channel.
On test 5, display control faults (marked *) can be fully checked out with the procedure given below.

Display and reset check

Connect an oscilloscope to the emitter of VT7 on the logic board, and set the counter controls as follows:

FUNCTION switch	-	TEST
GATE switch	-	AUTO
MEMORY switch	-	OFF
DISPLAY TIME	-	mid-travel
TIME BASE	-	position 5

Operate the RESET switch; the oscilloscope should show one of the following:

A. Voltage rises to a maximum and then falls sharply (see a. below).

B. A continuous repetition of A occurs (see b. below).

C. The voltage does not rise (see c. below).

D. The voltage does not fall (see d. below).

NOTE:. The time taken for the voltage to rise to a maximum depends on the setting of the DISPLAY TIME control.

The length of time that the voltage remains at minimum depends on the setting of the TIME BASE switch.

a. This may be accompanied by a non-repeated reading; this indicates faulty reset circuits.

Perform the checks indicated in Tables 5.2 and 5.3.

Table 5.2

Monitoring point	Level	Check, if any level incorrect
IC6 pin 13 (S12)	high (negative pulse)	IC24 pin 1: high (low)
IC7 pin 3 (S16)	low (positive pulse)	pin 2: high (pulse)
IC23 pin 8	low (positive pulse)	pin 3: low (high)
		pin 8: high (low)
		pin 9: low (high)
		pin 10: low (high)
		pin 11: high (pulse)
		pin 12: low (high)
		pin 13: high (low)

Conditions in brackets occur when RESET operated

Table 5.3

Monitoring point	Level	Check, if either level incorrect
IC22 pin 4	low (high)	IC6 pin 4: low
IC22 pin 9	high	pin 5: low (high)
		pin 6: high (high)
		pin 8: high (low)
		pin 9: high (pulse and low)
		pin 10: low (high)
		pin 11: low (high)
		pin 12: high (low)
		pin 13: high (low)

Conditions in brackets occur when RESET operated.

b. Bistable IC23b and c is not being reset by the sharp fall in voltage. Check levels as indicated in Table 5.4.

Table 5.4

Monitoring point	Level
IC23 pin 1	High (negative pulse from VT7 on reset)
pin 2	low
pin 3	low (positive pulse on reset)

c. In this case check that the level on IC23 pin 3 is low. If it is, check VT6; if it is not check as in b. above.

If IC23 pins 1 and 2 are low there may be no positive pulse from VT4. Checks levels as indicated in Table 5.5.

d. Check that the DISPLAY TIME control is not at ∞.

Check VT7, VT8 and associated components.

Check that levels on IC22 pins 3, 4, 5 and 8 are high and those on pins 9, 10 and 11 are low.

5.4 CALIBRATION AND TEST

5.4.1 Test equipment

a) Oscilloscope with x10 probe; 50 MHz bandwidth, e. g. M.I. TF 2210.

b) Signal generator; 50 MHz, e.g. M.I. TF 144H.

c) R.F. millivoltmeter, e.g. M.I. TF 2603.

d) Multimeter.

e) T connector, TM 7948 (optional accessory for TF 2603).

f) T connector with BNC sockets.

g) 50 Ω load, TM 7967 (optional accessory for TF 2603).

5.4.2 Power Supply

(circuit diagram, Fig. 7.5)

Test equipment: d.

Connect the instrument to the mains supply.

Check that the 2 A fuse, FS2, on the board is all right.

WARNING: Pin 15 on the board is at +200 V.

Supply lines

Connect the multimeter, set to 10 V d.c., to pin 1. The voltage measured should be between 5.1 V and 5.3 V.

If the voltage falls outside these values reselect R6 to bring it within limits; R6 should be between 8.2 kΩ and 33 kΩ.

Check that the other supply lines are as shown in Table 5.1.

5.4.3 +11 V supply – A amplifier

(circuit diagram, Fig. 7.2)

Test equipment: d.

Connect the multimeter between the emitter of VT3 and earth (i.e. between the R29 tag nearest C6, and pin 2). The meter should indicated +11 V ±0.1 V; if it does not, select R1 to bring the voltage within limits. R1 should be between 6.8 kΩ and 33 kΩ.

Table 5.5

Monitoring point	Level	Check, if level incorrect
VT1 base	high	S9 or S13 may not be present. Check as in Table 5.2.
VT2 collector	low	S9 or S13 going low will cause these states to change, allowing VT2c to go high, and VT3 and VT4 to oscillate.
VT4 collector	low	

5.4.4 A amplifier input circuit
(circuit diagram, Fig. 7.2)

Test equipment: d.

Before resistors R14 and R19 can be selected the pinch-off voltage (Vp) of the FET (VT5) must be known.

Temperature coefficient

R14 is selected to give minimum temperature coefficient of the input stage.

When the pinch-off voltage has been found, subtract 1 V from it, and select R14 so that this voltage (Vp-1) is across the resistor when the instrument is switched on. R14 should be between 1 kΩ and 8.2 kΩ.

Differential amplifier response

R19 is selected so that the collector currents of VT7 and VT8 are approximately 10 mA.

The resistance can be calculated from the equation

$$R19 = \frac{Vp - 1.7}{20}\ k\Omega$$

5.4.5 Trigger level
(circuit diagrams, Figs. 7.1 and 7.2)

Test equipment: b, c, d, e, f, g.

Negative trigger level excursion

On the amplifier board check that the voltage across R19 is approximately Vp -1.4, where Vp is the pinch-off voltage of VT5.

If necessary select R22 to achieve this voltage; the value of the resistor can be found from the equation

$$R22 = \frac{Vp - 1.4}{4}\ k\Omega$$

Trigger level range

Connect the test equipment as shown in Fig. 4.4 and set the controls as follows:

Signal generator:	Function	- CW
	Frequency	- 100 kHz
	Output level	- 2 V
Voltmeter:	Range	- 1 V
TF 2411:	Function	- FREQ A
	Time base	- position 3
	Gate	- AUTO
	Memory	- ON
	Display time	- minimum
	Trigger level controls	- fully counter-clockwise

Set the signal generator output level to 710 mV as monitored by the voltmeter and adjust RV4 until counting just occurs.

Rotate the TRIGGER LEVEL A controls fully clockwise. Set the signal generator output to the lowest level which will give a consistent reading on the counter. This level, monitored on the voltmeter, should be between 565 mV and 848 mV. If necessary readjust RV4 to get this result.

Rotate the TRIGGER LEVEL A controls fully counter-clockwise and repeat the above.

Auto trigger

With the test equipment set up as above, switch the TF 2411 TRIGGER LEVEL, FINE control to AUTO TRIGGER.

Set the signal generator output to 15 mV r.m.s. as monitored on the voltmeter. Adjust RV5 to the middle of the range over which a consistent reading is given on the counter.

Trigger backlash

Disconnect the input from the counter and set the controls as follows:

Function	-	COUNT A
Time base	-	position 3
Gate	-	OPEN
Display time	-	minimum
Trigger level	-	FINE control fully counter-clockwise but not switched to AUTO.

Rotate the coarse TRIGGER LEVEL A control from fully clockwise. The counter readout should increase by one count at about mid-travel of the control; leave the coarse control at this point.

Slowly rotate the FINE trigger level control to the point where the instrument triggers to give one count. Slight adjustment, back and forward, of the control should give a series of single counts.

If a burst of counting occurs, R44 is too low in value and should be changed.

Now connect a signal to the A channel socket and check that the instrument counts with an input of 10 mV. If a higher input is required it indicates that R44 is of too high a value.

5.4.6 Schmitt trigger

(circuit diagram, Fig. 7.2)

R29 is selected so that the Schmitt trigger, VT12 and VT13, is just on the point of operating when the collector potentials of VT10 and VT11 are equal.

The resistor should never require changing once it has been selected in calibration.

Chapter 6

Replaceable parts

Introduction

This section lists replaceable parts in alpha-numerical order of circuit reference. A separate list is given for each printed board, and those components associated with the chassis are listed at the beginning. The following abbreviations are used:

C : capacitor
Carb : carbon
Cer : ceramic
Elec : electrolytic
FS : fuse
IC : integrated circuit
ILP : indicator lamp
L : inductor
Met : metal
MR : semiconductor diode
Ox : oxide
PL : plug
Plas : plastic
R : resistor
RV : variable resistor
S : switch
SK : socket
T : transformer
TE : total excursion
V : valve
VT : transistor
W : watts at 70 °C
W* : watts at 55 °C
WW : wire wound
XL : crystal
† : value selected during test; nominal value shown.

Unless otherwise shown, all carbon resistors have a tolerance of ±10% and are rated at $\frac{1}{4}$ W at 70 °C.

Ordering

Orders for replacement parts should be sent to our Service Division at the address on the back cover. Specify the following information for each part required:

1. Type and serial number of instrument.
2. Circuit reference.
3. Description.
4. M.I. code number.

If a part is not listed state its function, location and description when ordering.

Circuit reference	Description	M.I. code
Main chassis		
C3	Plas 0.1µF 10% 250V d.c.	26512-220
C4	Elec 10µF +100-20% 35V	26414-121
C5	Cer 22pF ±0.25pF 750V d.c.	26324-715
ILP1		23735-291
ILP2		23735-291
ILP3		23735-291
ILP4		23735-291
ILP5		23735-291
ILP6		23735-291
ILP7		23735-291
ILP8		23735-291
ILP9		23735-291
ILP10		23735-291
MR1	1N914	28336-676
R1	Carb 1kΩ	24341-280
R2	Carb 10kΩ	24341-310
R3	Carb 470Ω	24341-269
R4	Carb 470Ω	24341-269
R5	Carb 100kΩ	24341-335
RV1	1kΩ Fine (with SL) } Trigger level switch assembly	25676-369
RV2	1kΩ Coarse } Trigger level switch assembly	
RV3	1MΩ Display time (with SA)	25563-505
RV4	5kΩ	25886-619
RV5	10kΩ	25886-623
SA	Display time switch (part of RV3)	

Circuit reference	Description	M.I. code
SB	Gate switch SPDT	23462-252
SC	Reset switch SPDT	23462-253
SD	Memory switch SPDT	23462-252
SE	Scaling factor switch	44325-404
SF	Function switch	44325-425
SH	Time base switch	44325-807
SL	Auto trigger switch (part of RV1)	
SKA	'A' input (D.C.) BNC	23443-443
SKB	'A' input (A.C.) BNC	23443-443
SKC	'B' input BNC	23443-443
SKD	'C' input BNC	23443-443
SKF	Prescaler socket	23435-430
	Units display window	37553-902
	Readout display window	37553-706
Knobs:	Display	41141-108
	Trigger level, coarse	41141-605
	Trigger level, fine	41141-605
	Function	41141-206
	Time base	41141-206
	Scaling factor	41141-702
	Mains lead and plug	43122-017

Circuit reference	Description	M.I. code
C8	Elec 5µF +100-20% 15V d.c.	26414-113
C9	Cer 68pF 2% 750V d.c.	26324-868
C10	Cer 33pF 5% 750V d.c.	26324-822
C11	Elec 25µF +100-20% 18V d.c.	26417-141
C12	Cer 68pF 2% 750V d.c.	26324-868
C13	Cer 0.1µF +50-25% 30V d.c.	26383-031
C14	Cer 0.1µF +50-25% 30V d.c.	26383-031
C15	Cer 47pF 2% 750V d.c.	26324-833
C16	Cer 0.1µF +50-25% 30V d.c.	26383-031
C17	Cer 10pF ±0.25pF 750V d.c.	26324-709
C18	Cer 0.1µF +50-25% 30V d.c.	26383-031
C19	Cer 47pF 2% 750V d.c.	26324-833
C20	Cer 0.1µF +50-25% 30V d.c.	26383-031
C21	Elec 10µF +100-20% 6V d.c.	26414-120
C22	Cer 0.1µF +50-25% 30V d.c.	26383-031
C23	Cer 0.1µF +50-25% 30V d.c.	26383-031
C24	Cer 0.1µF +50-25% 30V d.c.	26383-031
C25	Cer 0.1µF +50-25% 30V d.c.	26383-031
C26	Cer 0.001µF +40-20% 500V d.c.	26383-242
C27	Cer 0.1µF +50-25% 30V d.c.	26383-031
IC1	SL702C	28461-303
L1	Coil assembly	44225-033
L2	Coil assembly	44225-033
L3	Coil assembly	44225-033

Amplifier board 44823-706

Circuit reference	Description	M.I. code
C1	Cer 0.1µF +50-25% 30V d.c.	26383-031
C2	Cer 22pF ±0.25pF 750V d.c.	26324-715
C3	Cer 0.1µF +50-25% 30V d.c.	26383-031
C4	Cer 0.1µF +50-25% 30V d.c.	26383-031
C5	Cer 33pF 5% 750V d.c.	26324-822
C6	Elec 25µF +100-20% 18V d.c.	26417-141
C7	Cer 0.1µF +50-25% 30V d.c.	26383-031
MR1	Z5B5.6	28371-434
MR2	Z5B9.1	28371-753
MR3	FRB109	44521-028
MR4	1N3064	28336-249
MR5	1N3064	28336-249
MR6	FRB109	44521-028
MR7	Z5B4.3	28371-313

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
MR8	AAZ13	28321-137
MR9	1N3064	28336-249
MR11	1N3064	28336-249
MR12	1N3064	28336-249
MR13	AAZ13	28321-137
MR14	1N3064	28336-249
MR15	1N3064	28336-249
MR16	AAZ13	28321-137

MR3 and MR6 selected for leakage current of 0.5mA at 10V.

Circuit reference	Description	M.I. code
R1 †	Met ox 15kΩ nominal	31-44823-706
R2	Met ox 2.2kΩ 7% TE $\frac{3}{8}$W*	24552-088
R3	Met ox 2.7kΩ 7% TE $\frac{3}{8}$W*	24552-092
R4	Carb 1kΩ	24341-280
R5	Carb 15kΩ	24341-314
R6	Carb 1kΩ	24341-280
R7	WW 33Ω 5% 1$\frac{1}{2}$W	25123-033
R8	WW 150Ω 5% 1$\frac{1}{2}$W	25123-054
R9	Met ox 2.2Ω 10% $\frac{3}{8}$W*	24582-560
R10	Carb 1kΩ	24341-280
R11	Carb 1kΩ	24341-280
R12	Carb 180kΩ	24341-341
R13	Carb 820kΩ	24341-361
R14 †	Carb 2.2kΩ nominal	41-44823-706
R15	Carb 2.2kΩ	24341-288
R16	Carb 330Ω	24341-263
R17	Carb 68Ω	24341-243
R18	Carb 15Ω	24341-224
R19 †	Carb 39Ω nominal	46-44823-706
R20	Carb 330Ω	24341-263
R21	Carb 68Ω	24341-243
R22 †	Carb 1kΩ nominal	47-44823-706
R23	Carb 2.2kΩ	24341-288
R24	Carb 10kΩ	24341-310
R25	Carb 1kΩ	24341-280
R26	Carb 68Ω	24341-243
R27	Carb 330Ω	24341-263
R28	Carb 15Ω	24341-224
R29 †	Carb 68Ω nominal	50-44823-706
R30	Carb 68Ω	24341-243
R31	Carb 330Ω	24341-263
R32	Carb 330Ω	24341-263
R33	Carb 100Ω	24341-250
R34	Carb 10Ω	24341-220
R35	Carb 680Ω	24341-276
R36	Carb 6.8kΩ	24341-308
R37	Carb 100Ω	24341-250
R38	Carb 330Ω	24341-263
R39	Carb 680Ω	24341-276
R40	Carb 10Ω	24341-220
R41	Carb 680Ω	24341-276
R42	Carb 1.5kΩ	24341-284
R43	Carb 3.3kΩ	24341-294
R44 †	Carb 68Ω nominal	57-44823-706
R45	Carb 220Ω	24341-258
R46	Carb 470Ω	24341-269
R47	Carb 150Ω	24341-254
R48	Carb 470Ω	24341-269
R49	Carb 33Ω	24341-233
R50	Carb 100Ω	24341-250
R51	Carb 10kΩ	24341-310
R52	Carb 10kΩ	24341-310
R53	Carb 330Ω	24341-263
R54	Carb 220Ω	24341-258
R55	Carb 22Ω	24341-228
R56	Carb 820Ω	24341-278
R57	Carb 10kΩ	24341-310
R58	Carb 330Ω	24341-263
R59	Carb 22Ω	24341-228
R60	Carb 220Ω	24341-258
R61	Carb 820Ω	24341-278
R62	Carb 47kΩ	24341-326
R63	Carb 4.7kΩ	24341-300

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
R64	Carb 1kΩ	24341-280
R65	Carb 3.3kΩ	24341-294
R66	Carb 4.7kΩ	24341-300
VT1	BC108	28452-787
VT2	BFY51	28455-827
VT3	BFY51	28455-827
VT4	BCY72	28433-487
VT5	UC734	28459-006
VT6	MPS3640	28431-766
VT7	ZN3663	28451-692
VT8	ZN3663	28451-692
VT9	MPS3640	28431-766
VT10	MPS3640	28431-766
VT11	MPS3640	28431-766
VT12	2N3663	28451-692
VT13	MPS3640	28431-766
VT14	2N3663	28451-692
VT15	2N3663	28451-692
VT16	MPS3640	28431-766
VT17	BSX20	28452-197
VT18	BSX20	28452-197
VT19	BSX20	28452-197
VT20	BSX20	28452-197
VT21	BC108	28452-787
VT22	BC108	28452-787

Count board 44844-613

C1	Cer 33pF 5% 750V	26324-822
C2	Cer 33pF 5% 750V	26324-822
C3	Cer 0.1μF +80-20% 10V	26382-214
C4	Cer 33pF 5% 750V	26324-822
C5	Cer 0.001μF +40-20% 500V	26383-242
C6	Cer 0.1μF +80-20% 10V	26382-214
C7	Cer 33pF 5% 750V	26324-822
C8	Cer 0.1μF +80-20% 10V	26382-214

Circuit reference	Description	M.I. code
IC1	MC1013P	28462-005
IC2	SN7470N	28462-004
IC3	SN7470N	28462-004
IC4	SN7470N	28462-004
IC5	U6B995979	28469-701
IC6	U6B996079	28465-001
IC7	SN7490N	28464-002
IC8	U6B995979	28469-701
IC9	U6B996079	28465-001
IC10	U6A995879X	28464-003
IC11	U6B995979	28469-701
IC12	U6B996079	28465-001
IC13	U6A995879X	28464-003
IC14	U6B995979	28469-701
IC15	U6B996079	28465-001
IC16	U6A995879X	28464-003
IC17	U6B995979	28469-701
IC18	U6B996079	28465-001
IC19	U6A995879X	28464-003
IC20	U6B995979	28469-701
IC21	U6B996079	28465-001
IC22	U6A995879X	28464-003
IC23	U6B995979	28469-701
IC24	U6B996079	28465-001
MR1	1N3064	28336-249
MR2	AAZ13	28321-137
MR4	1N3064	28336-249
MR5	1N3064	28336-249
MR6	1N3064	28336-249
MR7	1N3064	28336-249
MR8	1N3064	28336-249
MR9	1N3064	28336-249
MR10	1N3064	28336-249
MR11	1N3064	28336-249
PLB	+200V	35685-123

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
R1	Carb 100Ω	24341-250
R2	Carb 470Ω	24341-269
R3	Carb 470Ω	24341-269
R4	Carb 470Ω	24341-269
R5	Carb 330Ω	24341-263
R6	Carb 470Ω	24341-269
R7	Carb 470Ω	24341-269
R8	Carb 470Ω	24341-269
R9	Carb 330Ω	24341-263
R10	Carb 470Ω	24341-269
R11	Carb 470Ω	24341-269
R12	Carb 470Ω	24341-269
R13	Carb 1.5kΩ	24341-284
R14	Carb 2.2kΩ	24341-288
R15	Carb 470Ω	24341-269
R16	Carb 1kΩ	24341-280
R17	Carb 1kΩ	24341-280
R18	Carb 470Ω	24341-269
R19	Carb 470Ω	24341-269
R20	Carb 1kΩ	24341-280
R21	Met ox 180Ω 7% TE $\frac{3}{8}$W*	24552-056
R22	Met ox 82Ω 7% TE $\frac{3}{8}$W*	24552-046
R23	Met ox 470Ω 7% TE $\frac{3}{8}$W*	24552-069
R24	Carb 100Ω	24341-250
R25	Carb 1kΩ	24341-280
R26	Carb 1.8kΩ	24341-286
R27	Carb 470Ω	24341-269
R28	Carb 22kΩ	24341-318
R29	Carb 22kΩ	24341-318
R30	Carb 470kΩ	24341-269
R31	Carb 470Ω	24341-269
R32	Carb 1kΩ	24341-280
R33	Carb 22kΩ	24341-318
R34	Carb 22kΩ	24341-318
R35	Carb 22kΩ	24341-318
R36	Carb 22kΩ	24341-318
R37	Carb 22kΩ	24341-318
R38	Carb 1kΩ	24341-280

Circuit reference	Description	M.I. code
SKM	+200V	23232-201
SKP		23435-076
V1	Readout tube	28224-312
V2	Readout tube	28224-312
V3	Readout tube	28224-312
V4	Readout tube	28224-312
V5	Readout tube	28224-312
V6	Readout tube	28224-312
V7	Readout tube	28224-312
VT1	BSX20	28452-197
VT2	BSX20	28452-197
VT3	BSX20	28452-197
VT4	BSX20	28452-197
VT5	BC108	28452-787
VT6	BSX20	28452-197
VT7	BSX20	28452-197
VT8	BCY72	28433-487
VT9	BSX20	28452-197
VT10	MPS3640	28431-766
VT11	BSX20	28452-197
VT12	BC108	28452-787

Logic board 44844-612

C1	Cer 0.01μF +80-20% 100V d.c.	26383-055
C2	Cer 0.001μF +40-20% 500V d.c.	26383-242
C3	Cer 0.1μF +80-20% 10V d.c.	26382-214
C4	Elec 6.8μF 10% 35V d.c.	26487-275
C5	Cer 0.01μF +80-20% 100V d.c.	26383-055
C6	Cer 0.1μF +80-20% 10V d.c.	26382-214
C7	Plas 0.01μF 10% 400V d.c.	26512-204

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
C8	Cer 0.01μF +80-20% 100V d.c.	26383-055
C9	Cer 0.1μF +80-20% 10V d.c.	26382-214
IC1	6AD9936-9	28469-152
IC2	ZN346E	28466-312
IC3	SN7402N	28466-204
IC4	ZN262E	28466-315
IC5	ZN262E	28466-315
IC6	ZN246E	28466-314
IC7	SN7490N	28464-002
IC8	ZN246E	28466-314
IC9	ZN224E	28466-311
IC10	SN7490N	28464-002
IC11	SN7490N	28464-002
IC12	SN7490N	28464-002
IC13	ZN224E	28466-311
IC14	ZN224E	28466-311
IC15	SN7490N	28464-002
IC16	SN7490N	28464-002
IC17	SN7490N	28464-002
IC18	SN7490N	28464-002
IC19	ZN346E	28466-312
IC20	ZN224E	28466-311
IC21	ZN262E	28466-315
IC22	SN7472N	28462-003
IC23	MC824P	28466-203
IC24	ZN346E	28466-312
MR1	AAZ13	28321-137
MR2	AAZ13	28321-137
MR3	AAZ13	28321-137
MR4	1N914	28336-676
MR5	Z5B10	28371-843
MR6	1N914	28336-676
MR7	AAZ13	28321-137
MR8	1N914	28336-676
MR9	S3237G	28321-365
MR10	1N914	28336-676
MR11	1N914	28336-676
MR12	1N914	28336-676
MR13	1N914	28336-676
R1	Carb 120Ω	24341-252
R2	Carb 120Ω	24341-252
R3	Carb 120Ω	24341-252
R4	Carb 120Ω	24341-252
R5	Carb 120Ω	24341-252
R6	Carb 120Ω	24341-252
R7	Carb 120Ω	24341-252
R8	Carb 120Ω	24341-252
R9	Carb 120Ω	24341-252
R10	Carb 120Ω	24341-252
R11	Carb 120Ω	24341-252
R12	Carb 120Ω	24341-252
R13	Carb 120Ω	24341-252
R14	Carb 120Ω	24341-252
R15	Carb 120Ω	24341-252
R16	Carb 120Ω	24341-252
R17	Carb 120Ω	24341-252
R18	Carb 120Ω	24341-252
R19	Carb 120Ω	24341-252
R20	Carb 1kΩ	24341-280
R21	Carb 4.7kΩ	24341-300
R22	Carb 2.2kΩ	24341-288
R23	Carb 100kΩ	24341-335
R24	Carb 22kΩ	24341-318
R25	Carb 1kΩ	24341-280
R26	Carb 1kΩ	24341-280
R27	Carb 220Ω	24341-258
R28	Carb 22kΩ	24341-318
R29	Carb 470Ω	24341-269
R30	Carb 680Ω	24341-276
R31	Carb 1kΩ	24341-280

For symbols and abbreviations see introduction to this chapter.

Circuit reference	Description	M.I. code
R32	Carb 2.2kΩ	24341-288
R33	Carb 330Ω	24341-263
R34	Carb 10Ω	24341-220
R35	Carb 33kΩ	24341-322
R36	Carb 3.3kΩ	24341-294
R37	Carb 1kΩ	24341-280
R38	Carb 470Ω	24341-269
R39	Carb 2.2kΩ	24341-288
R40	Carb 4.7kΩ	24341-300
R41	Carb 4.7kΩ	24341-300
R42	Carb 1kΩ	24341-280
R43	Carb 330Ω	24341-263
R44	Carb 470Ω	24341-269
R45	Carb 680Ω	24341-276
R46	Carb 1kΩ	24341-280
R47	Carb 47Ω	24341-237
R48	Carb 10kΩ	24341-310
R49	Carb 10kΩ	24341-310
R50	Carb 2.2kΩ	24341-288
R51	Carb 1kΩ	24341-280
R52	Carb 10MΩ	24341-391
VT1	BC108	28452-787
VT2	BC108	28452-787
VT3	BC108	28452-787
VT4	BC108	28452-787
VT5	BSX20	28452-197
VT6	BC108	28452-787
VT7	2N2646	28487-801
VT8	BCY71	28435-235
VT9	BSX20	28452-197
VT10	BSX20	28452-197
VT11	BCY72	28433-487
VT12	BC108	28452-787
VT13	BC108	28452-787

Power supply 44823-111

Circuit reference	Description	M.I. code
C1	Elec 10000μF +50-20% 18V	26424-111
C2	Elec 2500μF +50-20% 35V	26424-109
C3	Elec 200μF +100-20% 6V d.c.	26423-333
C4	Elec 50μF +100-20% 25V d.c.	26423-317
C5	Elec 8μF +50-20% 200V d.c.	26417-474
C6	Elec 8μF +50-20% 200V d.c.	26417-474
C7	Elec 8μF +50-20% 200V d.c.	26417-474
C8	Elec 8μF +50-20% 200V d.c.	26417-474
C9	Elec 8μF +50-20% 200V d.c.	26417-474
C10	Elec 8μF +50-20% 200V d.c.	26417-474
C11	Cer 0.1μF +80-20% 10V d.c.	26382-214
C12	Cer 0.1μF +80-20% 10V d.c.	26382-214
C13	Elec 100μF +100-20% 6V d.c.	26417-154
FS1	500mA (slow blow) mains	23411-005
FS2	2A	23411-060
	Fuse holder for FS2	23416-151
MR1	1S923	28356-018
MR2	Z5B3.3	28371-208
MR3	398F	28356-523
MR4	398F	28356-523
MR5	398F	28356-523
MR6	398F	28356-523
MR7	1S923	28356-018
MR8	398F	28356-523
MR9	398F	28356-523
MR10	398F	28356-523
MR11	398F	28356-523
MR12	Z5B6.2	28371-483
MR13	Z5B6.2	28371-483
MR14	Z5B7.5	28371-603
MR15	398F	28356-523
MR16	10Z5.6T5	28371-431
MR17	398F	28356-523

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
PLA	Mains	23423-151
R1	Carb 150kΩ 10% ¼W	24342-139
R2	Carb 150Ω	24341-254
R3	Carb 330Ω 10% ½W	24342-063
R4	Carb 330Ω	24341-263
R5	Met ox 2.4kΩ 7% TE ⅜W*	24552-089
R6 †	Met ox 12kΩ nominal	20-44823-111
R7	Met ox 4.7kΩ 7% TE ⅜W*	24552-100
R8	Carb 2.2kΩ	24341-288
R9	Carb 680Ω	24341-276
R10	Carb 220Ω	24341-258
R11	Carb 470Ω	24341-269
R12	Carb 1kΩ	24341-280
R13	Carb 680Ω	24341-276
R14	Carb 0.3Ω Eureka wire	
SJ	SUPPLY switch DPDT	23462-258
T1	Mains transformer	43467-703
VT1	BC108	28452-787
VT2	BC108	28452-787
VT3	BC108	28452-787
VT4	BC108	28452-787
VT5	BC108	28452-787
VT6	BCY72	28433-487
VT8	2N3055	28456-567

External frequency standard TM 9890

C1	Cer 0.01μF +80-20% 100V d.c.	26383-055
C2	Cer 0.01μF +80-20% 100V d.c.	26383-055
C3	Cer 0.1μF +80-20% 10V d.c.	26382-214
C4	Cer 47pF 2% 750V d.c.	26324-833
C5	Plas 100pF ±2pF 125V d.c.	26516-241
C6	Cer 0.1μF +80-20% 10V d.c.	26382-214
C7	Cer 0.01μF +80-20% 100V d.c.	26383-055
C8	Cer 0.1μF +80-20% 10V d.c.	26382-214
C9	Cer 0.1μF +80-20% 10V d.c.	26382-214
C10	Cer 0.1μF +80-20% 10V d.c.	26382-214
L1	Screened inductor	44228-402
MR1	1N3064	28336-249
MR2	1N3064	28336-249
MR3	1N3064	28336-249
MR4	AAZ13	28321-137
MR5	1N914	28336-676
MR6	1N914	28336-676
MR7	AAZ13	28321-137
R1	Carb 3.3kΩ	24341-294
R2	Carb 6.8kΩ	24341-306
R3	Carb 6.8kΩ	24341-306
R4	Carb 680Ω	24341-276
R5	Carb 680Ω	24341-276
R6	Carb 4.7kΩ	24341-300
R7	Carb 680Ω	24341-276
R8	Carb 680Ω	24341-276
R9	Carb 220Ω	24341-258
R10	Carb 470Ω	24341-269
R11	Carb 47Ω	24341-237
R12	Carb 680Ω	24341-276
R13	Carb 2.2kΩ	24341-288

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
R14	Carb 1kΩ	24341-280
R15	Carb 2.2kΩ	24341-288
R16	Carb 68Ω	24341-243
R17	Carb 680Ω	24341-276
SKA	INPUT socket	23443-443
VT1	BSX20	28452-197
VT2	BSX20	28452-197
VT3	BSX20	28452-197
VT4	BCY72	28433-487
VT5	BSX20	28452-197
VT6	BSX20	28452-197

10 MHz Frequency standard TM 9888

C1	Air 3pF-14.5pF variable	26816-236
C2	Plas 33pF ±2pF 125V d.c.	26516-127
C3	Cer 0.1μF +80-20% 10V d.c.	26382-214
C4	Mica 200pF 1% 350V d.c.	26268-329
C5	Mica 200pF 1% 350V d.c.	26268-329
C6	Cer 0.01μF +80-20% 100V d.c.	26383-055
C7	Cer 0.01μF +80-20% 100V d.c.	26383-055
C8	Cer 0.1μF +80-20% 10V d.c.	26382-214
C9	Cer 0.1μF +80-20% 10V d.c.	26382-214
C10	Cer 0.1μF +80-20% 10V d.c.	26382-214
MR1	1N3064	28336-249
MR2	1N3064	28336-249
MR3	1N3064	28336-249
MR4	1N914	28336-676
MR5	AAZ13	28321-137

Circuit reference	Description	M.I. code
R1	Carb 22kΩ	24341-318
R2	Carb 22kΩ	24341-318
R3	Carb 33Ω	24341-233
R4	Carb 1kΩ	24341-280
R5	Carb 680Ω	24341-276
R6	Carb 680Ω	24341-276
R7	Carb 6.8kΩ	24341-306
R8	Carb 3.3kΩ	24341-294
R9	Carb 6.8kΩ	24341-306
R10	Carb 2.2kΩ	24341-288
R11	Carb 68Ω	24341-243
R12	Carb 680Ω	24341-276
SA	INT/EXT switch SPDT	23462-252
SKA	INPUT socket BNC	23443-443
VT1	BSX20	28452-197
VT2	BSX20	28452-197
VT3	BSX20	28452-197
XL1	Crystal	28311-916

Internal frequency standard, TM 9933

C1	Cer 0.01μF +80-20% 100V d.c.	26383-055
C2	Cer 0.1μF +50-20% 30V d.c.	26383-031
C4	Plas 100pF ±2pF 125V d.c.	26516-241
C5	Cer 0.1μF +50-20% 30V d.c.	26383-031
C6	Cer 0.01μF +80-20% 100V d.c.	26383-055
C7	Elec 25μF +100-20% 25V d.c.	26423-311

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
R1	Met film 82Ω 2% ¼W	24638-225
R2	Carb 1kΩ	24341-280
R3	Carb 1kΩ	24341-280
R4	Carb 270Ω	24341-261
R5	Carb 220Ω	24341-258
R6	Carb 680Ω	24341-276
R7	Carb 100Ω	24341-250
R8	Carb 330Ω	24341-263
R9	Carb 1kΩ	24341-280
R10	Met ox 560Ω 5% ¼W	24581-234
R11	Met ox 470Ω 5% ¼W	24581-232
R12 †	Carb 1.5kΩ nominal	47-46821-005
R13	WW 150Ω 5% 1½W	25123-054
RV1	WW 10kΩ variable	25886-623
VT1	BC108	28452-787
VT2	BSX20	28452-197
VT3	BC108	28452-787
VT4	BC108	28452-787
VT5	MJE521	28454-806
VT6	BCY72	28433-487
XL1	Miniature crystal oscillator	28313-822

For symbols and abbreviations see introduction to this chapter

Chapter 7

Circuit diagrams

Circuit notes

1. COMPONENT VALUES

Resistors: no suffix = ohms, k = kilohms, M = megohms.
Capacitors: no suffix = microfarads, p = picofarads.
Inductors: no suffix = henry, m = millihenry, μ = microhenry.
: value selected during test, nominal value shown.

2. VOLTAGES

Printed in italics. Voltages are d.c. and relative to chassis unless otherwise indicated. Measured with a 20 kΩ/V meter.

arrow indicates voltage source points.

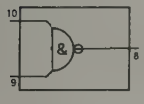
3. SYMBOLS

arrow indicates clockwise rotation of knob.

FUNCTION panel marking.

printed board tag.

main signal path.



integrated circuit (whole or part) showing function performed inside the rectangle, and pin numbers outside.

Logic lines

L1	C + S
L2	$\overline{\text{MP1 + MP2 + S}}$
L3	$\overline{\text{F + C + P.S. + A/B-C + LF}}$
L4	MP1 + MP2
L5	MP2
L6	P + S + T
L7	P + MP2 + S + T
L8	TEST + F + P.S. + LF
L9	P + T
L10	S
L11	TEST + MP1
L12	T + A/B-C
L13	P
L14	TEST + F + MP1 + MP2 + P.S. + LF
L15	$\overline{\text{P.S.}}$
L16	LF

Time Base lines

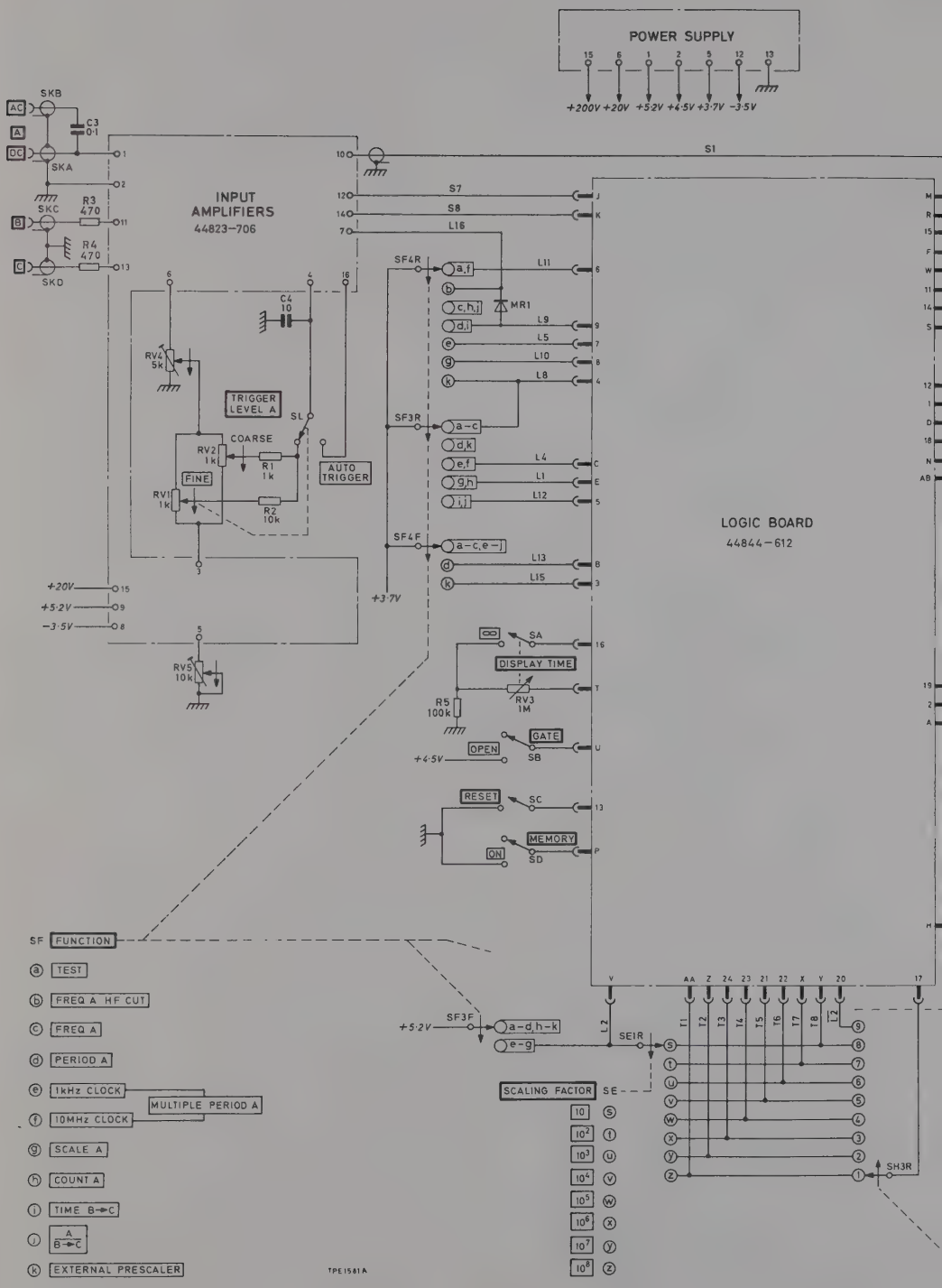
T1	10 s period
T2	1 s period
T3	100 ms period
T4	10 ms period
T5	1 ms period
T6	100 µs period
T7	10 µs period
T8	1 µs period
T9	0.1 µs period

Key to logic lines

LF	Freq. A, H.F. cut
F	Freq. A
P	Period A
MP1	Mult. period A, 10 MHz clock
MP2	Mult. period A, 1 kHz clock
S	Scale A
C	Count A
T	Time B-C
P.S.	External prescaler

Signal lines

S1	A input from amplifier
S2	A output to logic board
S3	Gate signal
S4	Count time base
S5	Time base to prescaler
S6	Time base from prescaler
S7	B signal
S8	C signal
S9	Gate 'Q' output
S10	10 MHz standard
S11	Gate 'preset'
S12	Gate 'clear'
S13	Gate latch
S14	Memory transfer
S15	Reset count chain
S16	Reset time base
S17	$\overline{\text{Count}}$
S18	Print command
S19	Inhibit


POWER SUPPLY
+200V +20V +5·2V +4·5V +3·7V −3·5V
INPUT AMPLIFIERS
44823–706
LOGIC BOARD
44844–612
SKB
SKA
SKC
SKD
R3 470
R4 470
C3 0·1
C4 10
RV4 5k
TRIGGER LEVEL A
SL
COARSE
FINE
RV2 1k
RV1 1k
R1 1k
R2 10k
AUTO TRIGGER
RV5 10k
SF4R
SF3R
SF4F
MR1
S1
S7
S8
L16
L11
L9
L5
L10
L8
L4
L1
L12
L13
L15
+3·7V
+20V
+5·2V
−3·5V
SA
DISPLAY TIME
RV3 1M
R5 100k
GATE
OPEN
SB
+4·5V
RESET
SC
MEMORY
ON
SD
SF FUNCTION
a TEST
b FREQ A HF CUT
c FREQ A
d PERIOD A
e 1kHz CLOCK
f 10MHz CLOCK
MULTIPLE PERIOD A
g SCALE A
h COUNT A
i TIME B→C
j A / B→C
k EXTERNAL PRESCALER
SF3F
SE1R
SCALING FACTOR SE
SH3R
TPE1581A

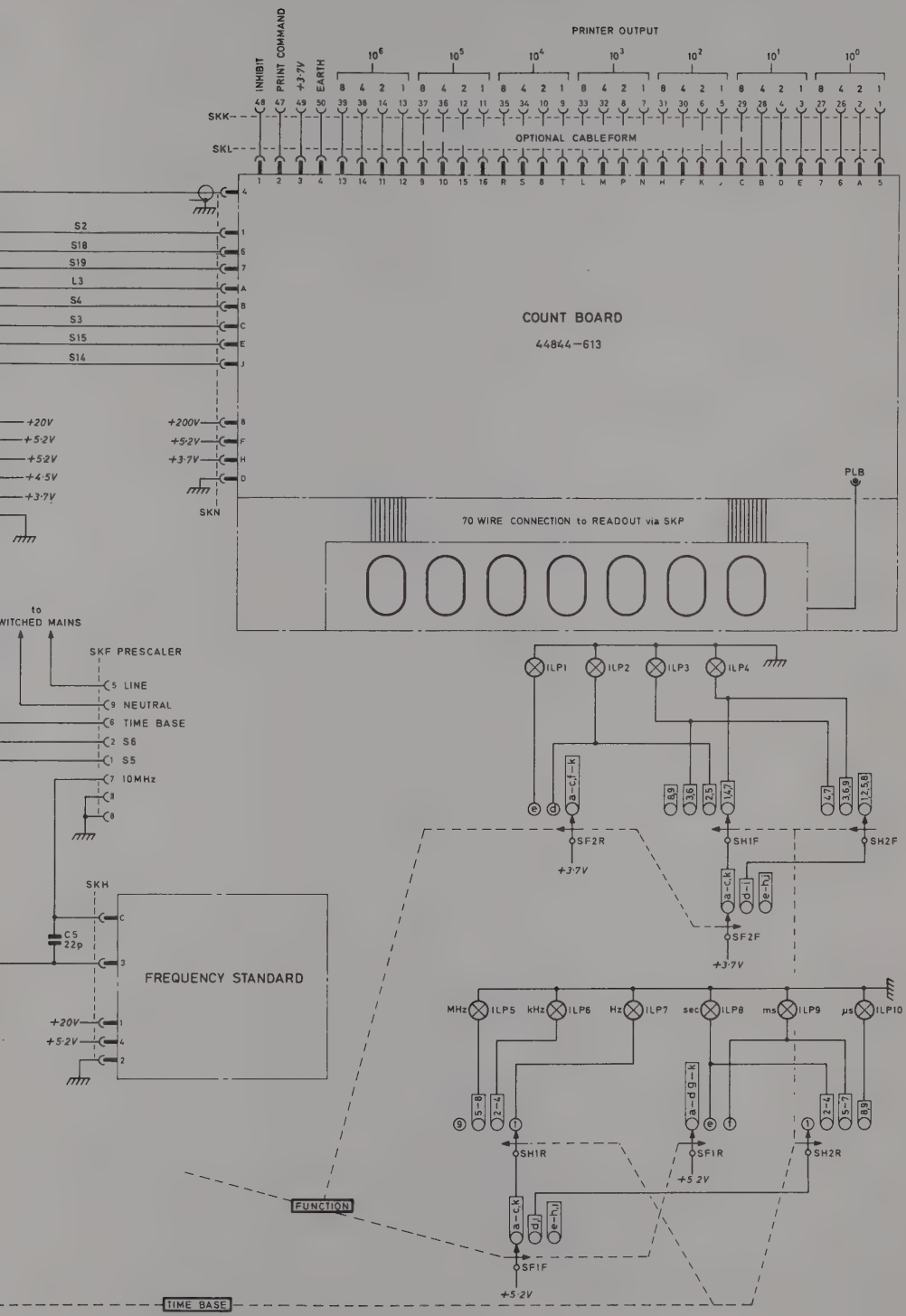
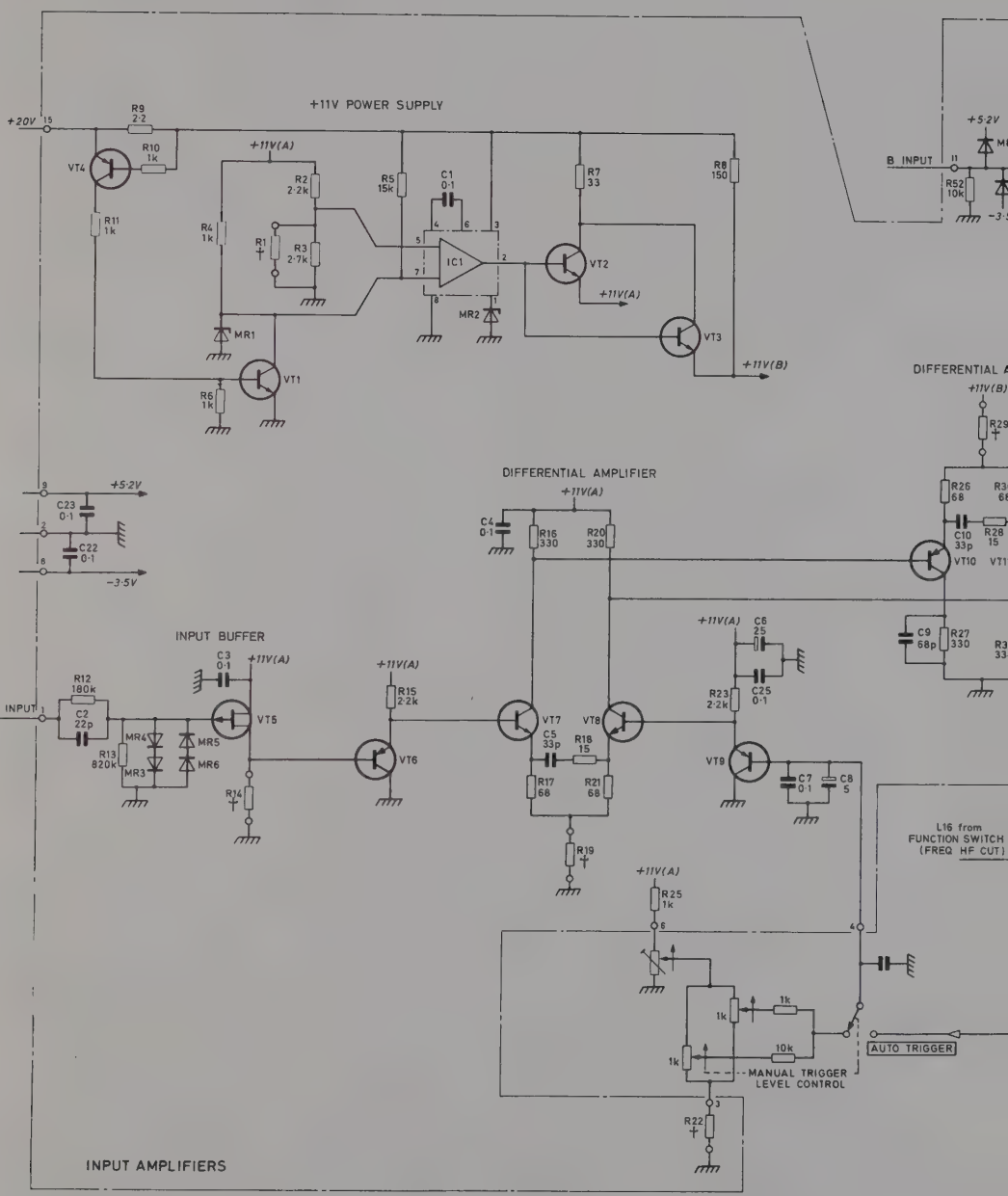


Fig. 7.1 Interconnecting diagram


+11V POWER SUPPLY
+20V
R9 2·2
VT4
R10 1k
+11V(A)
R11 1k
R2 2·2k
R5 15k
C1 0·1
R7 33
R8 150
R4 1k
R1
R3 2·7k
IC1
VT2
+11V(A)
MR2
MR1
VT3
+11V(B)
VT1
R6 1k
B INPUT
+5·2V
R52 10k
-3·5V
DIFFERENTIAL A
+11V(B)
R29
+5·2V
C23 0·1
C22 0·1
-3·5V
DIFFERENTIAL AMPLIFIER
+11V(A)
C4 0·1
R16 330
R20 330
R26 68
C10 33p
R28 15
VT10
VT11
INPUT BUFFER
C3 0·1
+11V(A)
+11V(A)
+11V(A)
C6 25
R12 180k
A INPUT
C2 22p
VT5
MR4
MR5
R15 2·2k
R23 2·2k
C25 0·1
C9 68p
R27 330
R13 820k
MR3
MR6
VT6
VT7
VT8
C5 33p
R18 15
VT9
C7 0·1
C8 5
R14
R17 68
R21 68
R19
L16 from FUNCTION SWITCH (FREQ HF CUT)
+11V(A)
R25 1k
1k
1k
10k
1k
AUTO TRIGGER
MANUAL TRIGGER LEVEL CONTROL
R22
INPUT AMPLIFIERS

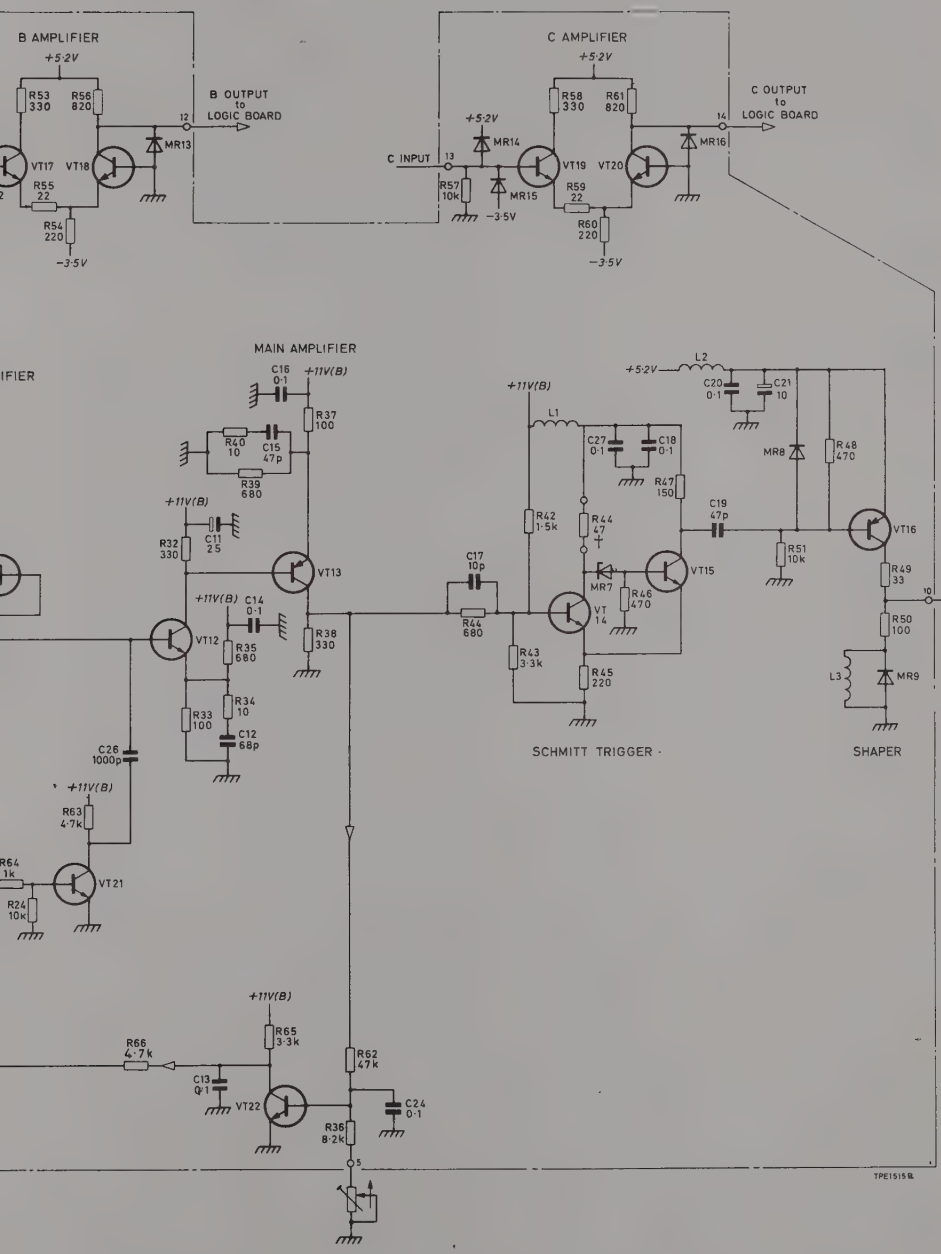
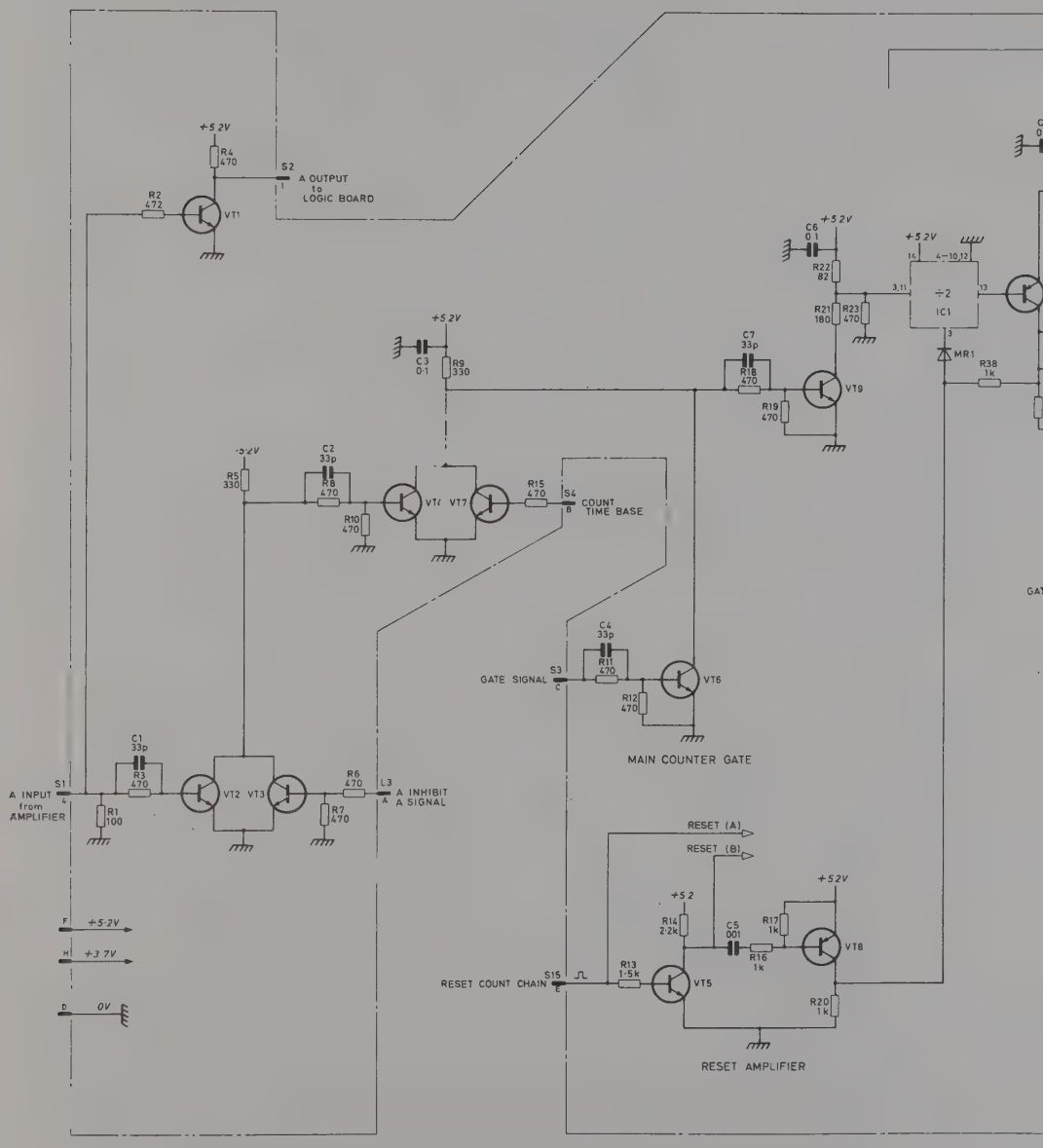


Fig. 7.2 Amplifier board


+5·2V
R4 470
S2
A OUTPUT to LOGIC BOARD
R2 472
VT1
C6 0·1
R22 82
R21 180
R23 470
÷2 IC1
MR1
R38 1k
C3 0·1
R9 330
C7 33p
R18 470
VT9
R19 470
C2 33p
R8 470
R5 330
R10 470
VT4 VT7
R15 470
S4
COUNT TIME BASE
C4 33p
R11 470
GATE SIGNAL
S3
VT6
R12 470
MAIN COUNTER GATE
C1 33p
R3 470
A INPUT from AMPLIFIER
S1
R1 100
VT2 VT3
R6 470
R7 470
L3
A INHIBIT A SIGNAL
RESET (A)
RESET (B)
+5·2V
+3·7V
0V
R14 2·2k
C5 001
R17 1k
R16 1k
VT8
R13 1·5k
S15
RESET COUNT CHAIN
VT5
R20 1k
RESET AMPLIFIER

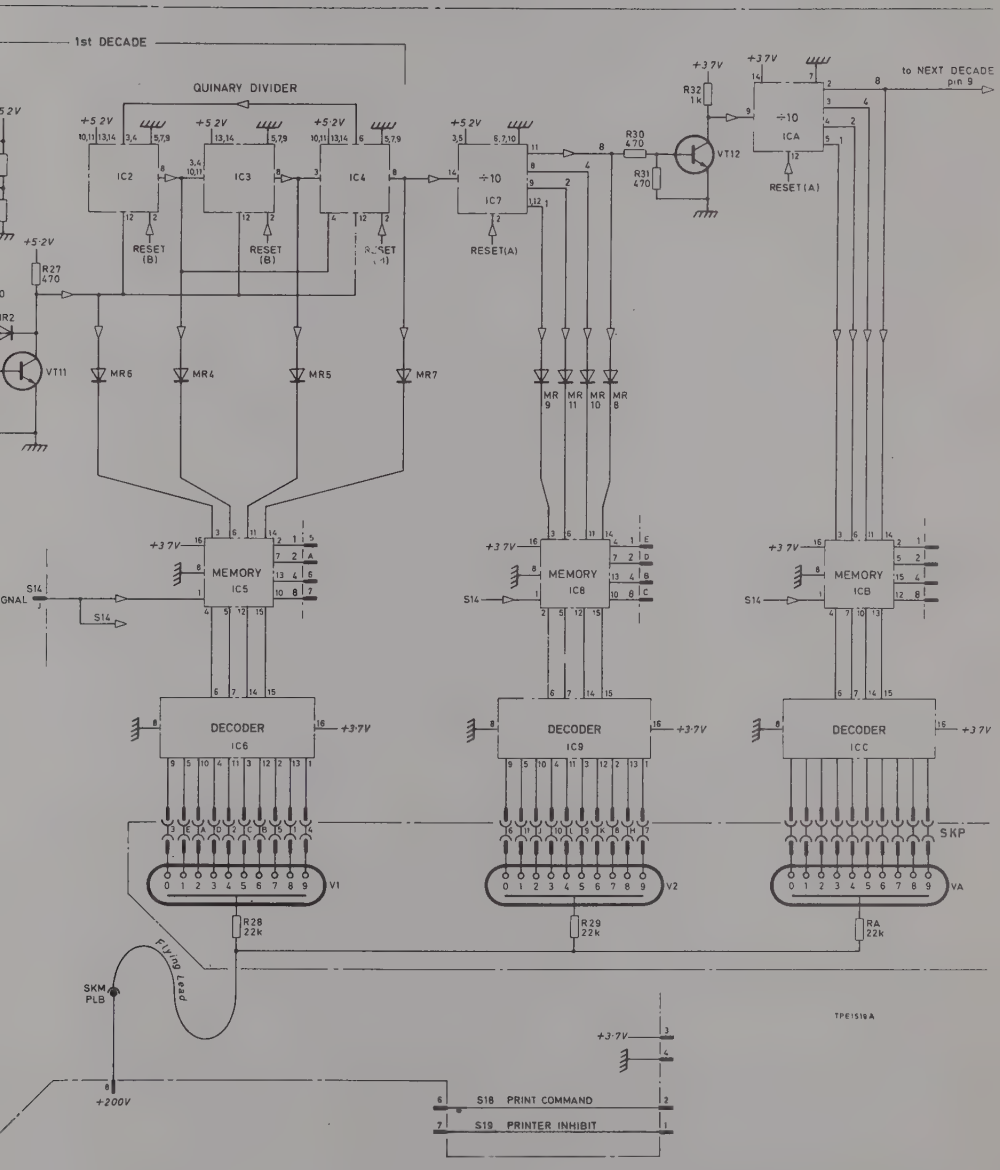
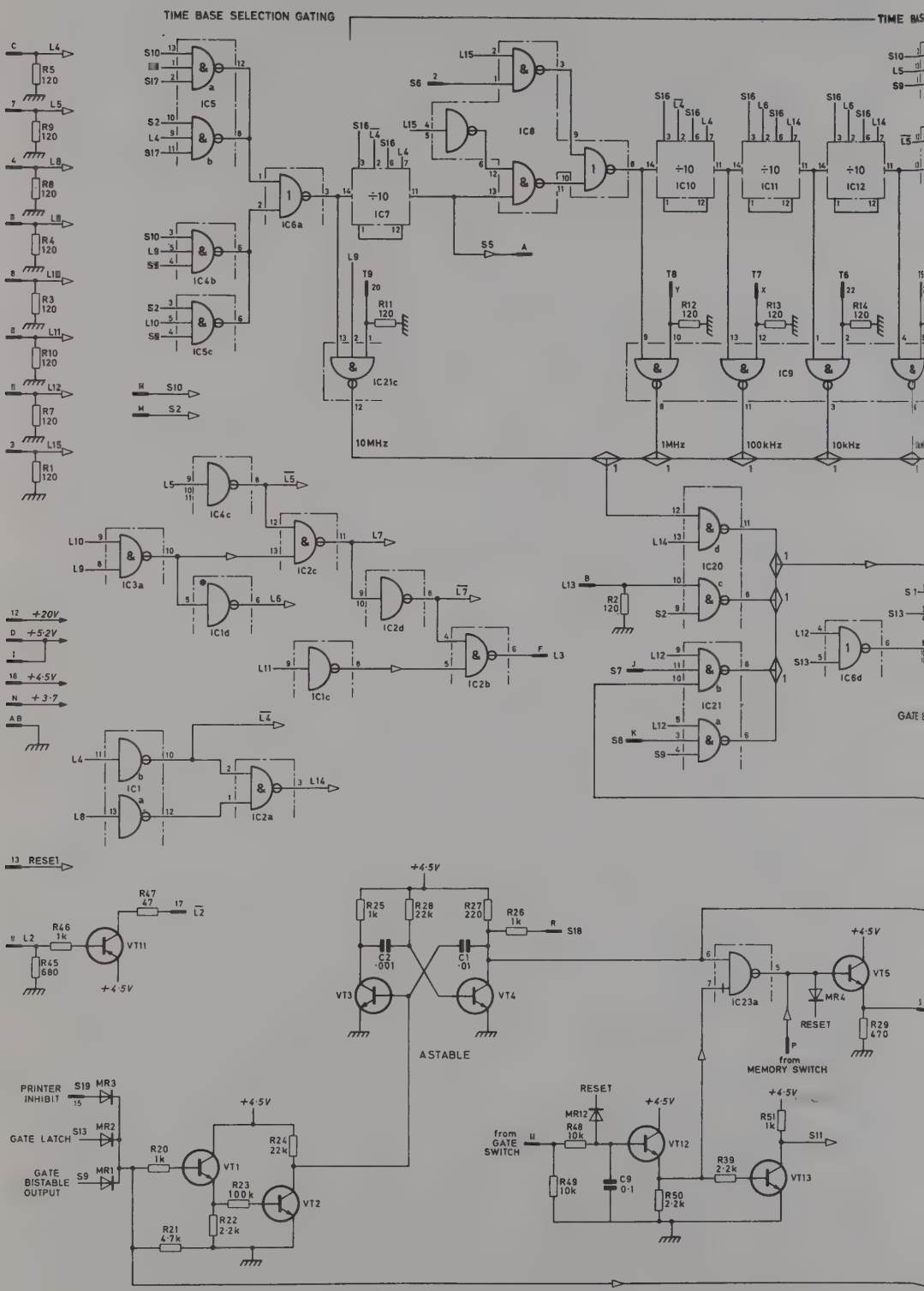


Fig. 7.3 Count board


TIME BASE SELECTION GATING
TIME BAS
IC5
IC6a
IC7
÷10
IC8
IC10
IC11
IC12
IC4b
IC5c
IC21c
IC9
10MHz
1MHz
100kHz
10kHz
IC4c
IC3a
IC2c
IC1d
IC2d
IC2b
IC1c
IC20
IC21
IC6d
IC1
IC2a
+20V
+5·2V
+4·5V
+3·7
RESET
ASTABLE
IC23a
VT1
VT2
VT3
VT4
VT5
VT11
VT12
VT13
PRINTER INHIBIT
GATE LATCH
GATE BISTABLE OUTPUT
from GATE SWITCH
from MEMORY SWITCH

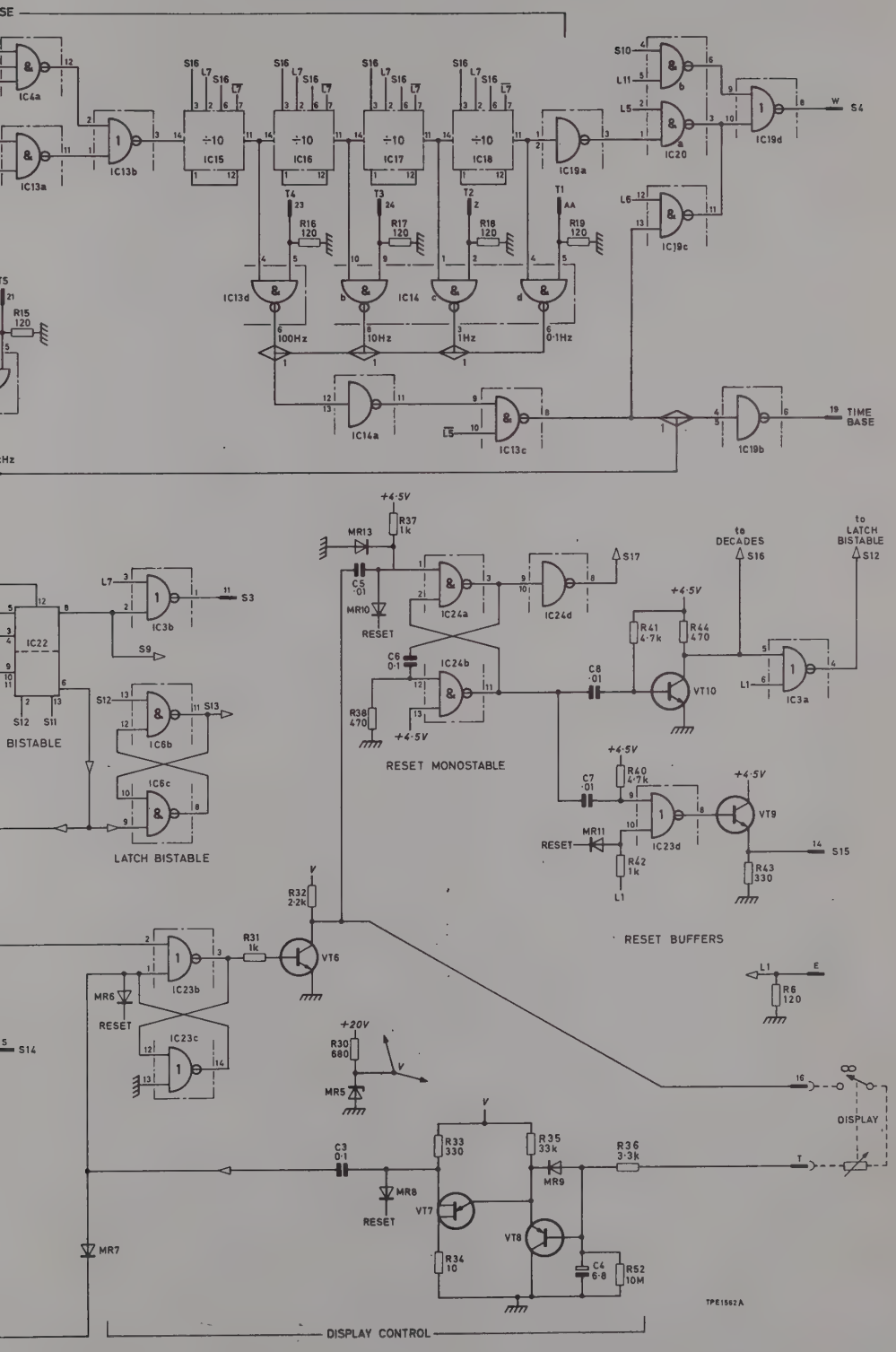
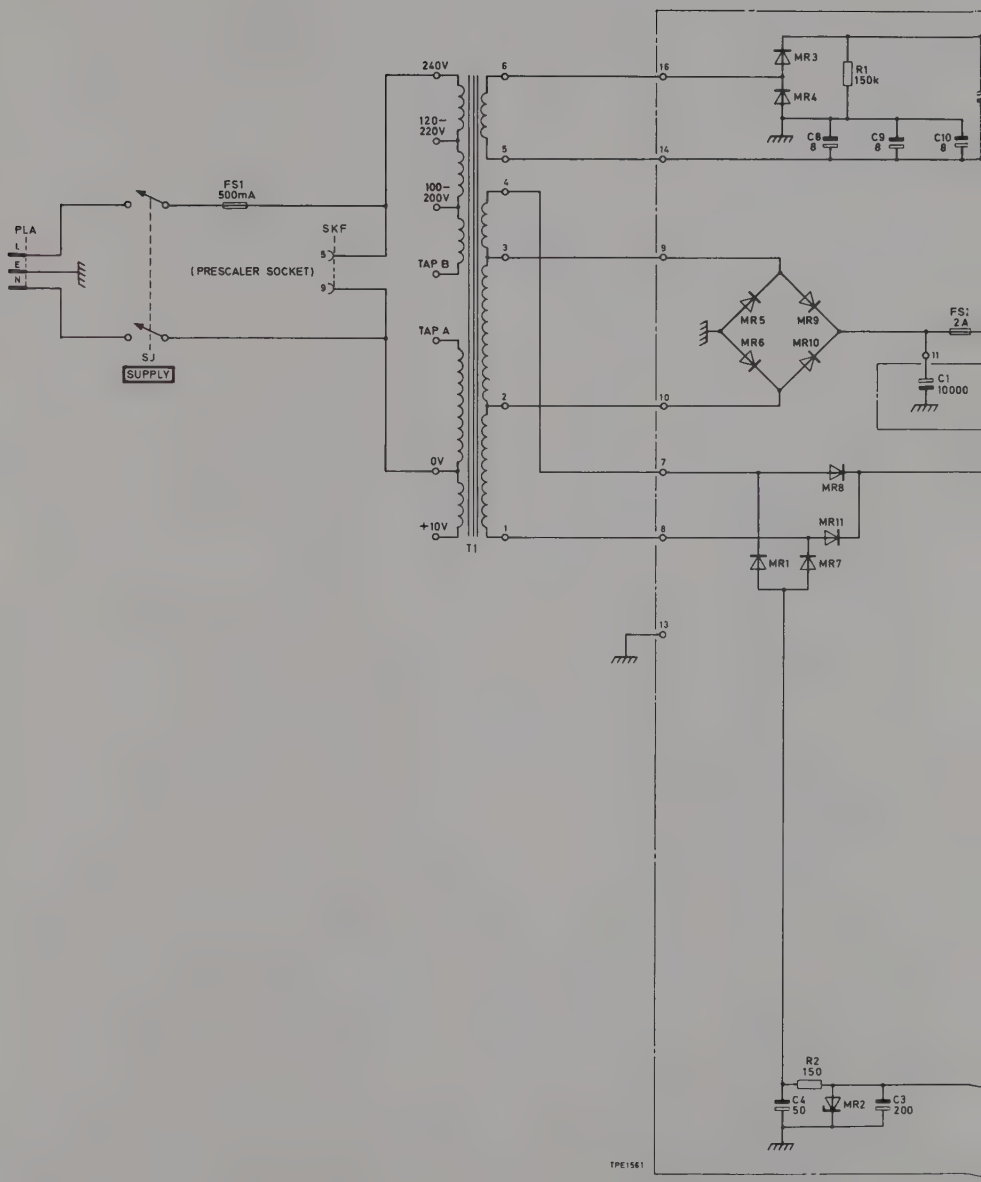


Fig. 7.4 Logic board


240V
120–220V
100–200V
TAP B
TAP A
0V
+10V
T1
FS1
500mA
PLA
L
E
N
SKF
5
9
(PRESCALER SOCKET)
SJ
SUPPLY
MR3
MR4
R1
150k
C8
8
C9
8
C10
8
MR5
MR9
MR6
MR10
FS:
2A
C1
10000
MR8
MR11
MR1
MR7
R2
150
C4
50
MR2
C3
200
TPE1561

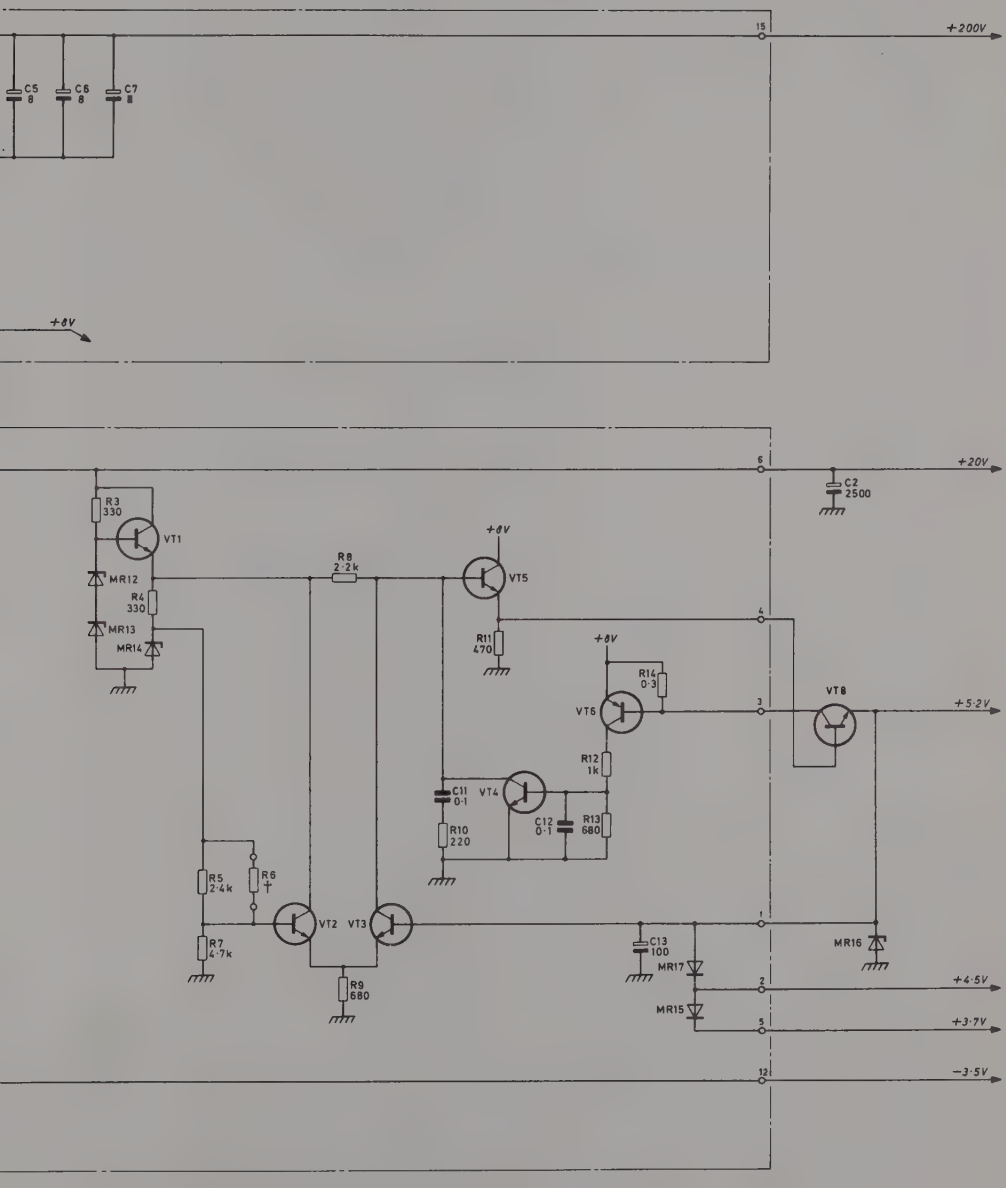
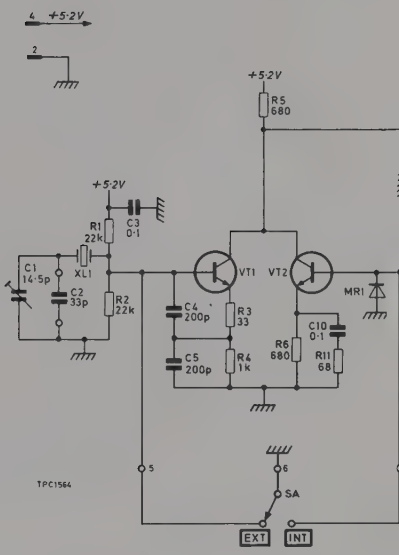
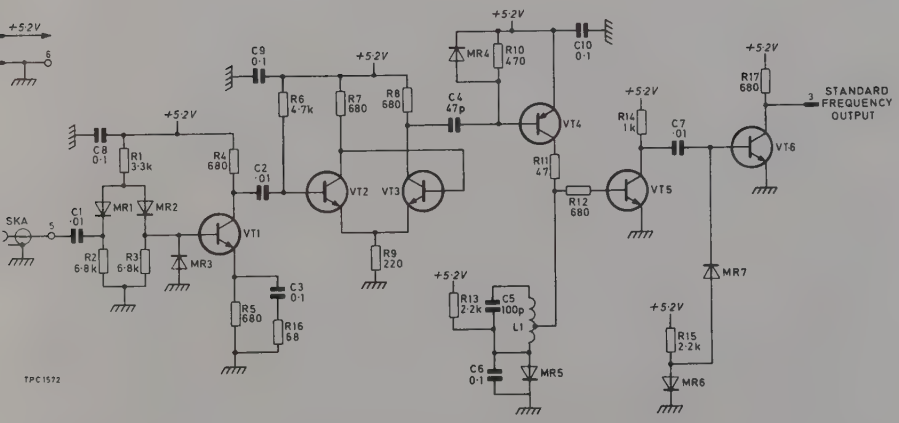


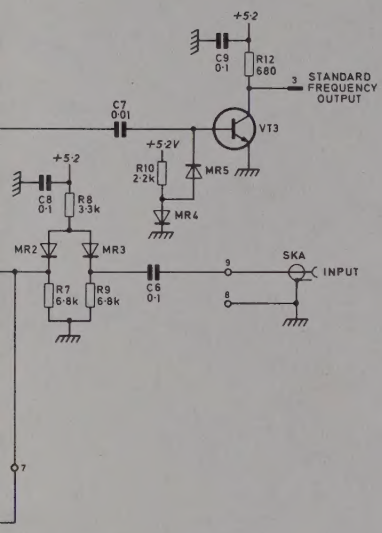
Fig. 7.5 Power supply

(a) 10 MHz standard: TM



(b) External frequency standard: TM 9890





(c) *Internal frequency standard: TM 9933*

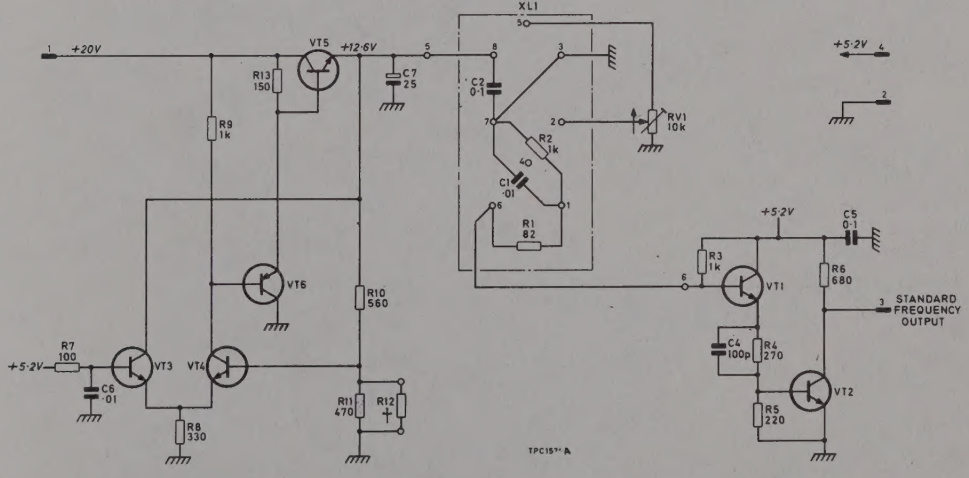


Fig. 7.6 Frequency standards

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